

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRR-b encoded:
				5 *
				6 * E795 VPKLS - Vector Pack Logical Saturate
				7 * E797 VPKS - Vector Pack Saturate
				8 * E7F8 VCEQ - Vector Compare Equal
				9 * E7F9 VCHL - Vector Compare High Logical
				10 * E7FB VCH - Vector Compare High
				11 *
				12 * James Wekel March 2025
				13 *****
				15 *****
				16 *
				17 * basic instruction tests
				18 *
				19 *****
				20 * This program tests proper functioning of the z/arch E7 VRR-b
				21 * Pack Logical Saturate, Pack Saturate, Compare, Compare Equal,
				22 * Compare High Logical instructions.
				23 * Exceptions are not tested.
				24 *
				25 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				26 * obvious coding errors. None of the tests are thorough. They are
				27 * NOT designed to test all aspects of any of the instructions.
				28 *
				29 *****
				30 *
				31 * *Testcase zvector-e7-16-PackCompare
				32 * *
				33 * * Zvector E7 instruction tests for VRR-b encoded:
				34 * *
				35 * * E795 VPKLS - Vector Pack Logical Saturate
				36 * * E797 VPKS - Vector Pack Saturate
				37 * * E7F8 VCEQ - Vector Compare Equal
				38 * * E7F9 VCHL - Vector Compare High Logical
				39 * * E7FB VCH - Vector Compare High
				40 * *
				41 * * # -----
				42 * * # This tests only the basic function of the instruction.
				43 * * # Exceptions are NOT tested.
				44 * * # -----
				45 * *
				46 * main size 2
				47 * numcpu 1
				48 * sysclear
				49 * archlvl z/Arch
				50 * *
				51 * loadcore "\$(testpath)/zvector-e7-16-PackCompare.core" 0x0
				52 * *
				53 * diag8cmd enable # (needed for messages to Hercules console)
				54 * runtest 5
				55 * diag8cmd disable # (reset back to default)
				56 * *

	57	*	*Done
	58	*	
	59	*	
	60	* * * * *	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
62				*****
63				* FCHECK Macro - Is a Facility Bit set?
64				*
65				* If the facility bit is NOT set, an message is issued and
66				* the test is skipped.
67				*
68				* Fcheck uses R0, R1 and R2
69				*
70				* eg. FCHECK 134, 'vector-packed-decimal'
71				*****
72				MACRO
73				FCHECK &BITNO, &NOTSETMSG
74	.	*		&BITNO : facility bit number to check
75	.	*		&NOTSETMSG : 'facility name'
76				LCLA &FBBYTE Facility bit in Byte
77				LCLA &FBBIT Facility bit within Byte
78				
79				LCLA &L(8)
80	&L(1)			SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
81				
82	&FBBYTE	SETA	&BITNO/8	
83	&FBBIT	SETA	&L((&BITNO-(&FBBYTE*8))+1)	
84	.	*	MNOTE	0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
85				
86			B	X&SYSNDX
87	*			Fcheck data area
88	*			skip messgae
89	SKT&SYSNDX DC	C'		Skipping tests: '
90		DC		C&NOTSETMSG
91		DC		C' (bit &BITNO) is not installed.'
92	SKL&SYSNDX EQU	*		- SKT&SYSNDX
93	*			facility bits
94		DS	FD	gap
95	FB&SYSNDX DS		4FD	
96		DS	FD	gap
97	*			
98	X&SYSNDX EQU	*		
99		LA		R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
100		STFLE		FB&SYSNDX get facility bits
101				
102		XGR		R0, R0
103		IC		R0, FB&SYSNDX+&FBBYTE get fbit byte
104		N		R0, =F' &FBBIT' is bit set?
105		BNZ		XC&SYSNDX
106	*			
107	*			facility bit not set, issue message and exit
108	*			
109		LA		R0, SKL&SYSNDX message length
110		LA		R1, SKT&SYSNDX message address
111		BAL		R2, MSG
112				
113		B		EOJ
114	XC&SYSNDX EQU	*		
115				MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				117	*****
				118	* Low core PSWs
				119	*****
00000000		00000000	0000A237	120	ZVE7TST START 0
		00000000		121	USING ZVE7TST, R0 Low core addressability
		00000140	00000000	122	
				123	SVOLDPSW EQU ZVE7TST+X' 140' z/Arch Supervisor call old PSW
00000000		00000000	000001A0	125	ORG ZVE7TST+X' 1A0' z/Architecture RESTART PSW
000001A0	00000001 80000000			126	DC X' 0000000180000000'
000001A8	00000000 00000200			127	DC AD(BEGIN)
000001B0		000001B0	000001D0	129	ORG ZVE7TST+X' 1D0' z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			130	DC X' 0002000180000000'
000001D8	00000000 0000DEAD			131	DC AD(X' DEAD')
000001E0		000001E0	00000200	133	ORG ZVE7TST+X' 200' Start of actual test program..
				135	*****
				136	* The actual "ZVE7TST" program itself...
				137	*****
				138	*
				139	* Architecture Mode: z/Arch
				140	* Register Usage:
				141	*
				142	* R0 (work)
				143	* R1- 4 (work)
				144	* R5 Testing control table - current test base
				145	* R6- R7 (work)
				146	* R8 First base register
				147	* R9 Second base register
				148	* R10 Third base register
				149	* R11 E7TEST call return
				150	* R12 E7TESTS register
				151	* R13 (work)
				152	* R14 Subroutine call
				153	* R15 Secondary Subroutine call or work
				154	*
				155	*****
00000200		00000200		157	USING BEGIN, R8 FIRST Base Register
00000200		00001200		158	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		159	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			161	BEGIN BALR R8, 0 Inititalize FIRST base register
00000202	0680			162	BCTR R8, 0 Inititalize FIRST base register
00000204	0680			163	BCTR R8, 0 Inititalize FIRST base register
00000206	4190 8800		00000800	165	LA R9, 2048(, R8) Inititalize SECOND base register
0000020A	4190 9800		00000800	166	LA R9, 2048(, R9) Inititalize SECOND base register
				167	

[illegible]

LOC	OBJECT CODE			ADDR1	ADDR2	STMT	
						243	*****
						244	* cc was not as expected
				0000031C	00000001	245	*****
						246	CCMSG EQU *
						247	*
						248	* is CS set by test?
						249	*
0000031C	E310	5008	0076		00000008	250	LB R1, M5 Get M5
00000322	E310	8360	0080		00000560	251	NG R1, =D' 1' isolate CS
00000328	4780	8100			00000300	252	BZ TESTREST not set?
						253	*
						254	* extract CC from extracted PSW
						255	*
0000032C	5810	500C			0000000C	256	L R1, CCPSW
00000330	8810	000C			0000000C	257	SRL R1, 12
00000334	5410	8370			00000570	258	N R1, =XL4' 3'
00000338	4210	5014			00000014	259	STC R1, CCFOUND save cc
						260	*
						261	* FILL IN MESSAGE
						262	*
0000033C	4820	5004			00000004	263	LH R2, TNUM get test number and convert
00000340	4E20	8ED6			000010D6	264	CVD R2, DECNUM
00000344	D211	8EC0	8EAA	000010C0	000010AA	265	MVC PRT3, EDIT
0000034A	DE11	8EC0	8ED6	000010C0	000010D6	266	ED PRT3, DECNUM
00000350	D202	8E65	8ECD	00001065	000010CD	267	MVC CCPRTNUM(3), PRT3+13 fill in message with test #
						268	
00000356	D207	8E82	5015	00001082	00000015	269	MVC CCPRTNAME, OPNAME fill in message with instruction
						270	
0000035C	B982	0022				271	XGR R2, R2 get CC as U8
00000360	4320	5009			00000009	272	IC R2, CC
00000364	4E20	8ED6			000010D6	273	CVD R2, DECNUM and convert
00000368	D211	8EC0	8EAA	000010C0	000010AA	274	MVC PRT3, EDIT
0000036E	DE11	8EC0	8ED6	000010C0	000010D6	275	ED PRT3, DECNUM
00000374	D200	8E98	8ECF	00001098	000010CF	276	MVC CCPRTEXP(1), PRT3+15 fill in message with CC field
						277	
0000037A	B982	0022				278	XGR R2, R2 get CCFOUND as U8
0000037E	4320	5014			00000014	279	IC R2, CCFOUND
00000382	4E20	8ED6			000010D6	280	CVD R2, DECNUM and convert
00000386	D211	8EC0	8EAA	000010C0	000010AA	281	MVC PRT3, EDIT
0000038C	DE11	8EC0	8ED6	000010C0	000010D6	282	ED PRT3, DECNUM
00000392	D200	8EA8	8ECF	000010A8	000010CF	283	MVC CCPRTGOT(1), PRT3+15 fill in message with ccfound
						284	
00000398	4100	0055			00000055	285	LA R0, CCPRTLNG message length
0000039C	4110	8E55			00001055	286	LA R1, CCPRTLNE messagfe address
000003A0	45F0	8236			00000436	287	BAL R15, RPTERROR
						288	
000003A4	5800	8374			00000574	289	L R0, =F' 1' set failed test indicator
000003A8	5000	8E00			00001000	290	ST R0, FAILED
						291	
000003AC	47F0	8100			00000300	292	B TESTREST
						293	

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT	
					295	*****
					296	* result not as expected:
					297	* issue message with test number, instruction under test
					298	* and instruction m4, m5
					299	*****
			000003B0	00000001	300	FAILMSG EQU *
000003B0	4820	5004		00000004	301	LH R2, TNUM get test number and convert
000003B4	4E20	8ED6		000010D6	302	CVD R2, DECNUM
000003B8	D211	8EC0 8EAA	000010C0	000010AA	303	MVC PRT3, EDIT
000003BE	DE11	8EC0 8ED6	000010C0	000010D6	304	ED PRT3, DECNUM
000003C4	D202	8E18 8ECD	00001018	000010CD	305	MVC PRTNUM(3), PRT3+13 fill in message with test #
					306	
000003CA	D207	8E33 5015	00001033	00000015	307	MVC PRTNAME, OPNAME fill in message with instruction
					308	
000003D0	B982	0022			309	XGR R2, R2 get M4 as U8
000003D4	4320	5007		00000007	310	IC R2, M4
000003D8	4E20	8ED6		000010D6	311	CVD R2, DECNUM and convert
000003DC	D211	8EC0 8EAA	000010C0	000010AA	312	MVC PRT3, EDIT
000003E2	DE11	8EC0 8ED6	000010C0	000010D6	313	ED PRT3, DECNUM
000003E8	D202	8E44 8ECD	00001044	000010CD	314	MVC PRTM4(3), PRT3+13 fill in message with M4 field
					315	
000003EE	B982	0022			316	XGR R2, R2 get M5 as U8
000003F2	4320	5008		00000008	317	IC R2, M5
000003F6	4E20	8ED6		000010D6	318	CVD R2, DECNUM and convert
000003FA	D211	8EC0 8EAA	000010C0	000010AA	319	MVC PRT3, EDIT
00000400	DE11	8EC0 8ED6	000010C0	000010D6	320	ED PRT3, DECNUM
00000406	D202	8E51 8ECD	00001051	000010CD	321	MVC PRTM5(3), PRT3+13 fill in message with M5 field
					322	
0000040C	4100	004D		0000004D	323	LA R0, PRTLNG message length
00000410	4110	8E08		00001008	324	LA R1, PRTLNE messagfe address
00000414	45F0	8236		00000436	325	BAL R15, RPTERROR
					327	*****
					328	* continue after a failed test
					329	*****
			00000418	00000001	330	FAILCONT EQU *
00000418	5800	8374		00000574	331	L R0, =F' 1' set failed test indicator
0000041C	5000	8E00		00001000	332	ST R0, FAILED
					333	
00000420	41C0	C004		00000004	334	LA R12, 4(0, R12) next test address
00000424	47F0	80D4		000002D4	335	B NEXTE7
					337	*****
					338	* end of testing; set ending psw
					339	*****
			00000428	00000001	340	ENDTEST EQU *
00000428	5810	8E00		00001000	341	L R1, FAILED did a test fail?
0000042C	1211				342	LTR R1, R1
0000042E	4780	8338		00000538	343	BZ EOJ No, exit
00000432	47F0	8350		00000550	344	B FAILTEST Yes, exit with BAD PSW

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				346	*****			
				347	*	RPTERROR	Report instruction test in error	
				348	*		R0 = MESSGAE LENGTH	
				349	*		R1 = ADDRESS OF MESSAGE	
				350	*****			
00000436	50F0 8254		00000454	352	RPTERROR	ST	R15, RPTSAVE	Save return address
0000043A	5050 8258		00000458	353		ST	R5, RPTSVR5	Save R5
				354	*			
				355	*	Use Hercules Diagnose for Message to console		
				356	*			
0000043E	9002 8260		00000460	357		STM	R0, R2, RPTDWSAV	save regs used by MSG
00000442	4520 8270		00000470	358		BAL	R2, MSG	call Hercules console MSG display
00000446	9802 8260		00000460	359		LM	R0, R2, RPTDWSAV	restore regs
0000044A	5850 8258		00000458	361		L	R5, RPTSVR5	Restore R5
0000044E	58F0 8254		00000454	362		L	R15, RPTSAVE	Restore return address
00000452	07FF			363		BR	R15	Return to caller
00000454	00000000			365	RPTSAVE	DC	F' 0'	R15 save area
00000458	00000000			366	RPTSVR5	DC	F' 0'	R5 save area
00000460	00000000 00000000			368	RPTDWSAV	DC	2D' 0'	R0-R2 save area for MSG call
				370	*****			
				371	*	Issue HERCULES MESSAGE pointed to by R1, length in R0		
				372	*	R2 = return address		
				373	*****			
00000470	4900 8378		00000578	375	MSG	CH	R0, =H' 0'	Do we even HAVE a message?
00000474	07D2			376		BNHR	R2	No, ignore
00000476	9002 82AC		000004AC	378		STM	R0, R2, MSGSAVE	Save registers
0000047A	4900 837A		0000057A	380		CH	R0, =AL2(L' MSGMSG)	Message length within limits?
0000047E	47D0 8286		00000486	381		BNH	MSGOK	Yes, continue
00000482	4100 005F		0000005F	382		LA	R0, L' MSGMSG	No, set to maximum
00000486	1820			384	MSGOK	LR	R2, R0	Copy length to work register
00000488	0620			385		BCTR	R2, 0	Minus-1 for execute
0000048A	4420 82B8		000004B8	386		EX	R2, MSGMVC	Copy message to O/P buffer
0000048E	4120 200A		0000000A	388		LA	R2, 1+L' MSGCMD(, R2)	Calculate true command length
00000492	4110 82BE		000004BE	389		LA	R1, MSGCMD	Point to true command
00000496	83120008			391		DC	X' 83' , X' 12' , X' 0008'	Issue Hercules Diagnose X' 008'
0000049A	4780 82A6		000004A6	392		BZ	MSGRET	Return if successful
				393				
0000049E	1222			394		LTR	R2, R2	Is Diag8 Ry (R2) 0?
000004A0	4780 82A6		000004A6	395		BZ	MSGRET	an error occurred but coninue
				396				
000004A4	0000			397		DC	H' 0'	CRASH for debugging purposes
000004A6	9802 82AC		000004AC	399	MSGRET	LM	R0, R2, MSGSAVE	Restore registers

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT	
					447	*=====
					448	*
					449	* NOTE: start data on an address that is easy to display
					450	* within Hercules
					451	*
					452	*=====
					453	
0000057C			0000057C	00001000	454	ORG ZVE7TST+X' 1000'
00001000	00000000				455	FAILED DC F' 0' some test failed?
00001004	00000000				456	TESTING DC F' 0' current test number
					458	*****
					459	* TEST failed : result messgae
					460	*****
					461	*
					462	* failed message and associated editting
					463	*
00001008	40404040	40404040			464	PRTLIN DC C' Test # '
00001018	A7A7A7				465	PRTNUM DC C' xxx'
0000101B	40868189	93858440			466	DC C' failed for instruction '
00001033	A7A7A7A7	A7A7A7A7			467	PRTNAME DC CL8' xxxxxxxxx'
0000103B	40A689A3	884094F4			468	DC C' with m4='
00001044	A7A7A7				469	PRTM4 DC C' xxx'
00001047	6B				470	DC C' , '
00001048	40A689A3	884094F5			471	DC C' with m5='
00001051	A7A7A7				472	PRTM5 DC C' xxx'
00001054	4B				473	DC C' . '
			0000004D	00000001	474	PRTLNG EQU *- PRTLIN
					475	
					476	*****
					477	* TEST failed : CC message
					478	*****
					479	*
					480	* failed message and associated editting
					481	*
00001055	40404040	40404040			482	CCPRTLIN DC C' Test # '
00001065	A7A7A7				483	CCPRTNUM DC C' xxx'
00001068	40A69996	95874083			484	DC c' wrong cc for instruction '
00001082	A7A7A7A7	A7A7A7A7			485	CCPRTNAME DC CL8' xxxxxxxxx'
0000108A	4085A797	8583A385			486	DC C' expected: cc='
00001098	A7				487	CCPRTEXP DC C' x'
00001099	6B				488	DC C' , '
0000109A	40998583	8589A585			489	DC C' received: cc='
000010A8	A7				490	CCPRTGOT DC C' x'
000010A9	4B				491	DC C' . '
			00000055	00000001	492	CCPRTLNG EQU *- CCPRTLIN

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				494	*****
				495	* TEST failed : message working storge
				496	*****
000010AA	40212020	20202020		497	EDIT DC XL18' 4021202020202020202020202020202020'
				498	
000010BC	7E7E7E6E			499	DC C' ==>'
000010C0	40404040	40404040		500	PRT3 DC CL18' '
000010D2	4C7E7E7E			501	DC C' <===''
000010D6	00000000	00000000		502	DECNUM DS CL16
				504	*****
				505	* Vector instruction results, pollution and input
				506	*****
000010E8				507	DS 0F
000010E8	00000000	00000000		508	DS XL16
000010F8	FFFFFFFF	FFFFFFFF		509	V1FUDGE DC XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF' V1 FUDGE
00001108	00000000	00000000		510	DS XL16
				512	*****
				513	* E7TEST DSECT
				514	*****
				516	E7TEST DSECT ,
00000000	00000000			517	TSUB DC A(0) pointer to test
00000004	0000			518	TNUM DC H' 00' Test Number
00000006	00			519	DC X' 00'
00000007	00			520	M4 DC HL1' 00' m4 used
00000008	00			521	M5 DC HL1' 00' m5 used
00000009	00			522	CC DC HL1' 00' cc expected
0000000A	00			523	CCMASK DC HL1' 00' not expected CC mask
				524	*
				525	* CC extrtaction
				526	*
0000000C	00000000	00000000		527	CCPSW DS 2F extract PSW after test (has CC)
00000014	00			528	CCFOUND DS X extracted cc
				529	
00000015	40404040	40404040		530	OPNAME DC CL8' ' E7 name
00000020	00000000			531	V1ADDR DC A(0) address of v1 result
00000024	00000000			532	V2ADDR DC A(0) address of v2 source
00000028	00000000			533	V3ADDR DC A(0) address of v3 source
0000002C	00000000			534	RELEN DC A(0) RESULT LENGTH
00000030	00000000			535	READDR DC A(0) result (expected) address
00000038	00000000	00000000		536	DS 2FD gap
00000048	00000000	00000000		537	V1OUTPUT DS XL16 V1 Output
00000058	00000000	00000000		538	DS 2FD gap
				539	
				540	* test routine will be here (from VRR-b macro)
				541	*
				542	* followed by
				543	* EXPECTED RESULT

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
00001118		00000000	0000A237	545 ZVE7TST CSECT , 546 DS OF	
				548 *****	
				549 * Macros to help build test tables	
				550 *****	
				552 *	
				553 * macro to generate individual test	
				554 *	
				555 MACRO	
				556 VRR_B &INST, &M4, &CC	
				557 . *	&INST - VRR-b instruction under test
				558 . *	&M4 - m4 field - element size
				559 . *	&CC - expected CC
				560	
				561 LCLA &XCC(4) &XCC has mask values for FAILED condition codes	
				562 &XCC(1) SETA 7 CC != 0	
				563 &XCC(2) SETA 11 CC != 1	
				564 &XCC(3) SETA 13 CC != 2	
				565 &XCC(4) SETA 14 CC != 3	
				566	
				567 GBLA &TNUM	
				568 &TNUM SETA &TNUM+1	
				569	
				570 DS OFD	
				571 USING *, R5	base for test data and test routine
				572	
				573 T&TNUM DC A(X&TNUM)	address of test routine
				574 DC H' &TNUM	test number
				575 DC X' 00'	
				576 DC HL1' &M4'	m4 used
				577 DC HL1' 1'	m5 used
				578 DC HL1' &CC'	CC
				579 DC HL1' &XCC(&CC+1)'	CC failed mask
				580	
				581 DS 2F	extracted PSW after test (has CC)
				582 DC X' FF'	extracted CC, if test failed
				583	
				584 DC CL8' &INST'	instruction name
				585 DC A(RE&TNUM)	address of v1 result
				586 DC A(RE&TNUM+16)	address of v2 source
				587 DC A(RE&TNUM+32)	address of v3 source
				588 DC A(16)	result length
				589 REA&TNUM DC A(RE&TNUM)	result address
				590 DS 2FD	gap
				591 V10&TNUM DS XL16	V1 output
				592 DS 2FD	gap
				593 . *	
				594 *	
				595 X&TNUM DS OF	
				596 LGF R1, V2ADDR	load v2 source
				597 VL v22, 0(R1)	use v21 to test decoder
				598 LGF R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				638	*****
				639	* E7 VRR-b tests
				640	*****
				641	PRINT DATA
				642	*
				643	*
				644	* E795 VPKLS - Vector Pack Logical Saturate
				645	* E797 VPKS - Vector Pack Saturate
				646	* E7F8 VCEQ - Vector Compare Equal
				647	* E7F9 VCHL - Vector Compare High Logical
				648	* E7FB VCH - Vector Compare High
				649	*
				650	* VRR-b instruction,
				651	* M, element size
				652	* CC expected condition code
				653	*
				654	* followed by
				655	* 16 byte V1 result
				656	* 16 byte V2 source
				657	* 16 byte V3 source
				658	*
				659	* NOTE: M5 is preset to 1; Condition Code Set (CS)
				660	*
				661	* -----
				662	* VPKLS - Vector Pack Logical Saturate
				663	* -----
				664	* cc=0: No saturation
				665	* cc=1: At least one but not all elements saturated
				666	* cc=3: Saturation on all elements
				667	* -----
				668	* case - simple cc debug
				669	* -----
				670	* Halfword
				671	VRR_B VPKLS, 1, 0
00001118				672+	DS 0FD
00001118		00001118		673+	USING *, R5
00001118	00001180			674+T1	DC A(X1)
0000111C	0001			675+	DC H' 1'
0000111E	00			676+	DC X' 00'
0000111F	01			677+	DC HL1' 1'
00001120	01			678+	DC HL1' 1'
00001121	00			679+	DC HL1' 0'
00001122	07			680+	DC HL1' 7'
00001124	00000000	00000000		681+	DS 2F
0000112C	FF			682+	DC X' FF'
0000112D	E5D7D2D3	E2404040		683+	DC CL8' VPKLS'
00001138	000011B0			684+	DC A(RE1)
0000113C	000011C0			685+	DC A(RE1+16)
00001140	000011D0			686+	DC A(RE1+32)
00001144	00000010			687+	DC A(16)
00001148	000011B0			688+REA1	DC A(RE1)
00001150	00000000	00000000		689+	DS 2FD
00001158	00000000	00000000			
00001160	00000000	00000000		690+V101	DS XL16
00001168	00000000	00000000			
00001170	00000000	00000000		691+	DS 2FD

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001178	00000000 00000000			692+*			
00001180				693+X1	DS	0F	
00001180	E310 5024 0014		00000024	694+	LGF	R1, V2ADDR	load v2 source
00001186	E761 0000 0806		00000000	695+	VL	v22, 0(R1)	use v21 to test decoder
0000118C	E310 5028 0014		00000028	696+	LGF	R1, V3ADDR	load v3 source
00001192	E771 0000 0806		00000000	697+	VL	v23, 0(R1)	use v22 to test decoder
00001198	E756 7010 1E95			698+	VPKLS	V21, V22, V23, 1, 1	test instruction
0000119E	B98D 0020			699+	EPSW	R2, R0	extract psw
000011A2	5020 500C		0000000C	700+	ST	R2, CCPSW	to save CC
000011A6	E750 5048 080E		00001160	701+	VST	V21, V101	save v1 output
000011AC	07FB			702+	BR	R11	return
000011B0				703+RE1	DC	0F	V1 for this test
000011B0				704+	DROP	R5	
000011B0	00000000 00000000			705	DC	XL16' 0000000000000000 0000000000000000'	result
000011B8	00000000 00000000						
000011C0	00000000 00000000			706	DC	XL16' 0000000000000000 0000000000000000'	v2
000011C8	00000000 00000000						
000011D0	00000000 00000000			707	DC	XL16' 0000000000000000 0000000000000000'	v3
000011D8	00000000 00000000						
				708			
				709	VRR_B	VPKLS, 1, 1	
000011E0				710+	DS	0FD	
000011E0		000011E0		711+	USING	*, R5	base for test data and test routine
000011E0	00001248			712+T2	DC	A(X2)	address of test routine
000011E4	0002			713+	DC	H' 2'	test number
000011E6	00			714+	DC	X' 00'	
000011E7	01			715+	DC	HL1' 1'	m4 used
000011E8	01			716+	DC	HL1' 1'	m5 used
000011E9	01			717+	DC	HL1' 1'	CC
000011EA	0B			718+	DC	HL1' 11'	CC failed mask
000011EC	00000000 00000000			719+	DS	2F	extracted PSW after test (has CC)
000011F4	FF			720+	DC	X' FF'	extracted CC, if test failed
000011F5	E5D7D2D3 E2404040			721+	DC	CL8' VPKLS'	instruction name
00001200	00001278			722+	DC	A(RE2)	address of v1 result
00001204	00001288			723+	DC	A(RE2+16)	address of v2 source
00001208	00001298			724+	DC	A(RE2+32)	address of v3 source
0000120C	00000010			725+	DC	A(16)	result length
00001210	00001278			726+REA2	DC	A(RE2)	result address
00001218	00000000 00000000			727+	DS	2FD	gap
00001220	00000000 00000000						
00001228	00000000 00000000			728+V102	DS	XL16	V1 output
00001230	00000000 00000000						
00001238	00000000 00000000			729+	DS	2FD	gap
00001240	00000000 00000000						
				730+*			
00001248				731+X2	DS	0F	
00001248	E310 5024 0014		00000024	732+	LGF	R1, V2ADDR	load v2 source
0000124E	E761 0000 0806		00000000	733+	VL	v22, 0(R1)	use v21 to test decoder
00001254	E310 5028 0014		00000028	734+	LGF	R1, V3ADDR	load v3 source
0000125A	E771 0000 0806		00000000	735+	VL	v23, 0(R1)	use v22 to test decoder
00001260	E756 7010 1E95			736+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001266	B98D 0020			737+	EPSW	R2, R0	extract psw
0000126A	5020 500C		0000000C	738+	ST	R2, CCPSW	to save CC
0000126E	E750 9028 080E		00001228	739+	VST	V21, V102	save v1 output
00001274	07FB			740+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001278				741+RE2	DC	0F	V1 for this test
00001278				742+	DROP	R5	
00001278	00000000 00000000			743	DC	XL16' 0000000000000000 0000000000000000'	result
00001280	FFFFFFFF FFFFFFFF						
00001288	00000000 00000000			744	DC	XL16' 0000000000000000 0000000000000000'	v2
00001290	00000000 00000000						
00001298	FFFFFFFF FFFFFFFF			745	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
000012A0	FFFFFFFF FFFFFFFF						
				746			
				747	VRR_B	VPKLS, 1, 3	
000012A8				748+	DS	0FD	
000012A8		000012A8		749+	USING	*, R5	base for test data and test routine
000012A8	00001310			750+T3	DC	A(X3)	address of test routine
000012AC	0003			751+	DC	H' 3'	test number
000012AE	00			752+	DC	X' 00'	
000012AF	01			753+	DC	HL1' 1'	m4 used
000012B0	01			754+	DC	HL1' 1'	m5 used
000012B1	03			755+	DC	HL1' 3'	CC
000012B2	0E			756+	DC	HL1' 14'	CC failed mask
000012B4	00000000 00000000			757+	DS	2F	extracted PSW after test (has CC)
000012BC	FF			758+	DC	X' FF'	extracted CC, if test failed
000012BD	E5D7D2D3 E2404040			759+	DC	CL8' VPKLS'	instruction name
000012C8	00001340			760+	DC	A(RE3)	address of v1 result
000012CC	00001350			761+	DC	A(RE3+16)	address of v2 source
000012D0	00001360			762+	DC	A(RE3+32)	address of v3 source
000012D4	00000010			763+	DC	A(16)	result length
000012D8	00001340			764+REA3	DC	A(RE3)	result address
000012E0	00000000 00000000			765+	DS	2FD	gap
000012E8	00000000 00000000						
000012F0	00000000 00000000			766+V103	DS	XL16	V1 output
000012F8	00000000 00000000						
00001300	00000000 00000000			767+	DS	2FD	gap
00001308	00000000 00000000						
				768+*			
00001310				769+X3	DS	0F	
00001310	E310 5024 0014		00000024	770+	LGF	R1, V2ADDR	load v2 source
00001316	E761 0000 0806		00000000	771+	VL	v22, 0(R1)	use v21 to test decoder
0000131C	E310 5028 0014		00000028	772+	LGF	R1, V3ADDR	load v3 source
00001322	E771 0000 0806		00000000	773+	VL	v23, 0(R1)	use v22 to test decoder
00001328	E756 7010 1E95			774+	VPKLS	V21, V22, V23, 1, 1	test instruction
0000132E	B98D 0020			775+	EPSW	R2, R0	extract psw
00001332	5020 500C		0000000C	776+	ST	R2, CCPSW	to save CC
00001336	E750 5048 080E		000012F0	777+	VST	V21, V103	save v1 output
0000133C	07FB			778+	BR	R11	return
00001340				779+RE3	DC	0F	V1 for this test
00001340				780+	DROP	R5	
00001340	FFFFFFFF FFFFFFFF			781	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00001348	FFFFFFFF FFFFFFFF						
00001350	FFFFFFFF FFFFFFFF			782	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001358	FFFFFFFF FFFFFFFF						
00001360	FFFFFFFF FFFFFFFF			783	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001368	FFFFFFFF FFFFFFFF						
				784			
				785 *Word			
				786	VRR_B	VPKLS, 2, 0	
00001370				787+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001370		00001370		788+	USING *, R5	base for test data and test routine
00001370	000013D8			789+T4	DC A(X4)	address of test routine
00001374	0004			790+	DC H' 4'	test number
00001376	00			791+	DC X' 00'	
00001377	02			792+	DC HL1' 2'	m4 used
00001378	01			793+	DC HL1' 1'	m5 used
00001379	00			794+	DC HL1' 0'	CC
0000137A	07			795+	DC HL1' 7'	CC failed mask
0000137C	00000000 00000000			796+	DS 2F	extracted PSW after test (has CC)
00001384	FF			797+	DC X' FF'	extracted CC, if test failed
00001385	E5D7D2D3 E2404040			798+	DC CL8' VPKLS'	instruction name
00001390	00001408			799+	DC A(RE4)	address of v1 result
00001394	00001418			800+	DC A(RE4+16)	address of v2 source
00001398	00001428			801+	DC A(RE4+32)	address of v3 source
0000139C	00000010			802+	DC A(16)	result length
000013A0	00001408			803+REA4	DC A(RE4)	result address
000013A8	00000000 00000000			804+	DS 2FD	gap
000013B0	00000000 00000000					
000013B8	00000000 00000000			805+V104	DS XL16	V1 output
000013C0	00000000 00000000					
000013C8	00000000 00000000			806+	DS 2FD	gap
000013D0	00000000 00000000					
				807+*		
000013D8				808+X4	DS 0F	
000013D8	E310 5024 0014		00000024	809+	LGF R1, V2ADDR	load v2 source
000013DE	E761 0000 0806		00000000	810+	VL v22, 0(R1)	use v21 to test decoder
000013E4	E310 5028 0014		00000028	811+	LGF R1, V3ADDR	load v3 source
000013EA	E771 0000 0806		00000000	812+	VL v23, 0(R1)	use v22 to test decoder
000013F0	E756 7010 2E95			813+	VPKLS V21, V22, V23, 2, 1	test instruction
000013F6	B98D 0020			814+	EPSW R2, R0	extract psw
000013FA	5020 500C		0000000C	815+	ST R2, CCPSW	to save CC
000013FE	E750 5048 080E		000013B8	816+	VST V21, V104	save v1 output
00001404	07FB			817+	BR R11	return
00001408				818+RE4	DC 0F	V1 for this test
00001408				819+	DROP R5	
00001408	00000000 00000000			820	DC XL16' 0000000000000000 0000000000000000'	result
00001410	00000000 00000000					
00001418	00000000 00000000			821	DC XL16' 0000000000000000 0000000000000000'	v2
00001420	00000000 00000000					
00001428	00000000 00000000			822	DC XL16' 0000000000000000 0000000000000000'	v3
00001430	00000000 00000000					
				823		
				824	VRR_B VPKLS, 2, 1	
00001438				825+	DS 0FD	
00001438		00001438		826+	USING *, R5	base for test data and test routine
00001438	000014A0			827+T5	DC A(X5)	address of test routine
0000143C	0005			828+	DC H' 5'	test number
0000143E	00			829+	DC X' 00'	
0000143F	02			830+	DC HL1' 2'	m4 used
00001440	01			831+	DC HL1' 1'	m5 used
00001441	01			832+	DC HL1' 1'	CC
00001442	0B			833+	DC HL1' 11'	CC failed mask
00001444	00000000 00000000			834+	DS 2F	extracted PSW after test (has CC)
0000144C	FF			835+	DC X' FF'	extracted CC, if test failed
0000144D	E5D7D2D3 E2404040			836+	DC CL8' VPKLS'	instruction name
00001458	000014D0			837+	DC A(RE5)	address of v1 result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000145C	000014E0			838+	DC	A(RE5+16)	address of v2 source
00001460	000014F0			839+	DC	A(RE5+32)	address of v3 source
00001464	00000010			840+	DC	A(16)	result length
00001468	000014D0			841+REA5	DC	A(RE5)	result address
00001470	00000000 00000000			842+	DS	2FD	gap
00001478	00000000 00000000						
00001480	00000000 00000000			843+V105	DS	XL16	V1 output
00001488	00000000 00000000						
00001490	00000000 00000000			844+	DS	2FD	gap
00001498	00000000 00000000						
				845+*			
000014A0				846+X5	DS	0F	
000014A0	E310 5024 0014		00000024	847+	LGF	R1, V2ADDR	load v2 source
000014A6	E761 0000 0806		00000000	848+	VL	v22, 0(R1)	use v21 to test decoder
000014AC	E310 5028 0014		00000028	849+	LGF	R1, V3ADDR	load v3 source
000014B2	E771 0000 0806		00000000	850+	VL	v23, 0(R1)	use v22 to test decoder
000014B8	E756 7010 2E95			851+	VPKLS	V21, V22, V23, 2, 1	test instruction
000014BE	B98D 0020			852+	EPSW	R2, R0	extract psw
000014C2	5020 500C		0000000C	853+	ST	R2, CCPSW	to save CC
000014C6	E750 5048 080E		00001480	854+	VST	V21, V105	save v1 output
000014CC	07FB			855+	BR	R11	return
000014D0				856+RE5	DC	0F	V1 for this test
000014D0				857+	DROP	R5	
000014D0	00000000 00000000			858	DC	XL16' 0000000000000000 FFFFFFFF'	result
000014D8	FFFFFFFF FFFFFFFF						
000014E0	00000000 00000000			859	DC	XL16' 0000000000000000 0000000000000000'	v2
000014E8	00000000 00000000						
000014F0	FFFFFFFF FFFFFFFF			860	DC	XL16' FFFFFFFF FFFFFFFF FFFFFFFF'	v3
000014F8	FFFFFFFF FFFFFFFF						
				861			
				862	VRR_B	VPKLS, 2, 3	
00001500				863+	DS	0FD	
00001500		00001500		864+	USING	*, R5	base for test data and test routine
00001500	00001568			865+T6	DC	A(X6)	address of test routine
00001504	0006			866+	DC	H' 6'	test number
00001506	00			867+	DC	X' 00'	
00001507	02			868+	DC	HL1' 2'	m4 used
00001508	01			869+	DC	HL1' 1'	m5 used
00001509	03			870+	DC	HL1' 3'	CC
0000150A	0E			871+	DC	HL1' 14'	CC failed mask
0000150C	00000000 00000000			872+	DS	2F	extracted PSW after test (has CC)
00001514	FF			873+	DC	X' FF'	extracted CC, if test failed
00001515	E5D7D2D3 E2404040			874+	DC	CL8' VPKLS'	instruction name
00001520	00001598			875+	DC	A(RE6)	address of v1 result
00001524	000015A8			876+	DC	A(RE6+16)	address of v2 source
00001528	000015B8			877+	DC	A(RE6+32)	address of v3 source
0000152C	00000010			878+	DC	A(16)	result length
00001530	00001598			879+REA6	DC	A(RE6)	result address
00001538	00000000 00000000			880+	DS	2FD	gap
00001540	00000000 00000000						
00001548	00000000 00000000			881+V106	DS	XL16	V1 output
00001550	00000000 00000000						
00001558	00000000 00000000			882+	DS	2FD	gap
00001560	00000000 00000000						
				883+*			
00001568				884+X6	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001568	E310 5024 0014		00000024	885+	LGF	R1, V2ADDR	load v2 source
0000156E	E761 0000 0806		00000000	886+	VL	v22, 0(R1)	use v21 to test decoder
00001574	E310 5028 0014		00000028	887+	LGF	R1, V3ADDR	load v3 source
0000157A	E771 0000 0806		00000000	888+	VL	v23, 0(R1)	use v22 to test decoder
00001580	E756 7010 2E95			889+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001586	B98D 0020			890+	EPSW	R2, R0	extract psw
0000158A	5020 500C		0000000C	891+	ST	R2, CCPSW	to save CC
0000158E	E750 5048 080E		00001548	892+	VST	V21, V106	save v1 output
00001594	07FB			893+	BR	R11	return
00001598				894+RE6	DC	0F	V1 for this test
00001598				895+	DROP	R5	
00001598	FFFFFFFF FFFFFFFF			896	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000015A0	FFFFFFFF FFFFFFFF						
000015A8	FFFFFFFF FFFFFFFF			897	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000015B0	FFFFFFFF FFFFFFFF						
000015B8	FFFFFFFF FFFFFFFF			898	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
000015C0	FFFFFFFF FFFFFFFF						
				899			
				900 *DoubleWord			
				901	VRR_B	VPKLS, 3, 0	
000015C8				902+	DS	0FD	
000015C8		000015C8		903+	USING	*, R5	base for test data and test routine
000015C8	00001630			904+T7	DC	A(X7)	address of test routine
000015CC	0007			905+	DC	H' 7'	test number
000015CE	00			906+	DC	X' 00'	
000015CF	03			907+	DC	HL1' 3'	m4 used
000015D0	01			908+	DC	HL1' 1'	m5 used
000015D1	00			909+	DC	HL1' 0'	CC
000015D2	07			910+	DC	HL1' 7'	CC failed mask
000015D4	00000000 00000000			911+	DS	2F	extracted PSW after test (has CC)
000015DC	FF			912+	DC	X' FF'	extracted CC, if test failed
000015DD	E5D7D2D3 E2404040			913+	DC	CL8' VPKLS'	instruction name
000015E8	00001660			914+	DC	A(RE7)	address of v1 result
000015EC	00001670			915+	DC	A(RE7+16)	address of v2 source
000015F0	00001680			916+	DC	A(RE7+32)	address of v3 source
000015F4	00000010			917+	DC	A(16)	result length
000015F8	00001660			918+REA7	DC	A(RE7)	result address
00001600	00000000 00000000			919+	DS	2FD	gap
00001608	00000000 00000000						
00001610	00000000 00000000			920+V107	DS	XL16	V1 output
00001618	00000000 00000000						
00001620	00000000 00000000			921+	DS	2FD	gap
00001628	00000000 00000000						
				922+*			
00001630				923+X7	DS	0F	
00001630	E310 5024 0014		00000024	924+	LGF	R1, V2ADDR	load v2 source
00001636	E761 0000 0806		00000000	925+	VL	v22, 0(R1)	use v21 to test decoder
0000163C	E310 5028 0014		00000028	926+	LGF	R1, V3ADDR	load v3 source
00001642	E771 0000 0806		00000000	927+	VL	v23, 0(R1)	use v22 to test decoder
00001648	E756 7010 3E95			928+	VPKLS	V21, V22, V23, 3, 1	test instruction
0000164E	B98D 0020			929+	EPSW	R2, R0	extract psw
00001652	5020 500C		0000000C	930+	ST	R2, CCPSW	to save CC
00001656	E750 5048 080E		00001610	931+	VST	V21, V107	save v1 output
0000165C	07FB			932+	BR	R11	return
00001660				933+RE7	DC	0F	V1 for this test
00001660				934+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001660	00000000 00000000			935	DC	XL16' 0000000000000000 0000000000000000'	result
00001668	00000000 00000000						
00001670	00000000 00000000			936	DC	XL16' 0000000000000000 0000000000000000'	v2
00001678	00000000 00000000						
00001680	00000000 00000000			937	DC	XL16' 0000000000000000 0000000000000000'	v3
00001688	00000000 00000000						
				938			
				939	VRR_B	VPKLS, 3, 1	
00001690				940+	DS	0FD	
00001690		00001690		941+	USING	*, R5	base for test data and test routine
00001690	000016F8			942+T8	DC	A(X8)	address of test routine
00001694	0008			943+	DC	H' 8'	test number
00001696	00			944+	DC	X' 00'	
00001697	03			945+	DC	HL1' 3'	m4 used
00001698	01			946+	DC	HL1' 1'	m5 used
00001699	01			947+	DC	HL1' 1'	CC
0000169A	0B			948+	DC	HL1' 11'	CC failed mask
0000169C	00000000 00000000			949+	DS	2F	extracted PSW after test (has CC)
000016A4	FF			950+	DC	X' FF'	extracted CC, if test failed
000016A5	E5D7D2D3 E2404040			951+	DC	CL8' VPKLS'	instruction name
000016B0	00001728			952+	DC	A(RE8)	address of v1 result
000016B4	00001738			953+	DC	A(RE8+16)	address of v2 source
000016B8	00001748			954+	DC	A(RE8+32)	address of v3 source
000016BC	00000010			955+	DC	A(16)	result length
000016C0	00001728			956+REA8	DC	A(RE8)	result address
000016C8	00000000 00000000			957+	DS	2FD	gap
000016D0	00000000 00000000						
000016D8	00000000 00000000			958+V108	DS	XL16	V1 output
000016E0	00000000 00000000						
000016E8	00000000 00000000			959+	DS	2FD	gap
000016F0	00000000 00000000						
				960+*			
000016F8				961+X8	DS	0F	
000016F8	E310 5024 0014		00000024	962+	LGF	R1, V2ADDR	load v2 source
000016FE	E761 0000 0806		00000000	963+	VL	v22, 0(R1)	use v21 to test decoder
00001704	E310 5028 0014		00000028	964+	LGF	R1, V3ADDR	load v3 source
0000170A	E771 0000 0806		00000000	965+	VL	v23, 0(R1)	use v22 to test decoder
00001710	E756 7010 3E95			966+	VPKLS	V21, V22, V23, 3, 1	test instruction
00001716	B98D 0020			967+	EPSW	R2, R0	extract psw
0000171A	5020 500C		0000000C	968+	ST	R2, CCPSW	to save CC
0000171E	E750 5048 080E		000016D8	969+	VST	V21, V108	save v1 output
00001724	07FB			970+	BR	R11	return
00001728				971+RE8	DC	0F	V1 for this test
00001728				972+	DROP	R5	
00001728	00000000 00000000			973	DC	XL16' 0000000000000000 FFFFFFFF'	result
00001730	FFFFFFFF FFFFFFFF						
00001738	00000000 00000000			974	DC	XL16' 0000000000000000 0000000000000000'	v2
00001740	00000000 00000000						
00001748	FFFFFFFF FFFFFFFF			975	DC	XL16' FFFFFFFF'	v3
00001750	FFFFFFFF FFFFFFFF						
				976			
				977	VRR_B	VPKLS, 3, 3	
00001758				978+	DS	0FD	
00001758		00001758		979+	USING	*, R5	base for test data and test routine
00001758	000017C0			980+T9	DC	A(X9)	address of test routine
0000175C	0009			981+	DC	H' 9'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000175E	00			982+	DC	X' 00'	
0000175F	03			983+	DC	HL1' 3'	m4 used
00001760	01			984+	DC	HL1' 1'	m5 used
00001761	03			985+	DC	HL1' 3'	CC
00001762	0E			986+	DC	HL1' 14'	CC failed mask
00001764	00000000 00000000			987+	DS	2F	extracted PSW after test (has CC)
0000176C	FF			988+	DC	X' FF'	extracted CC, if test failed
0000176D	E5D7D2D3 E2404040			989+	DC	CL8' VPKLS'	instruction name
00001778	000017F0			990+	DC	A(RE9)	address of v1 result
0000177C	00001800			991+	DC	A(RE9+16)	address of v2 source
00001780	00001810			992+	DC	A(RE9+32)	address of v3 source
00001784	00000010			993+	DC	A(16)	result length
00001788	000017F0			994+REA9	DC	A(RE9)	result address
00001790	00000000 00000000			995+	DS	2FD	gap
00001798	00000000 00000000						
000017A0	00000000 00000000			996+V109	DS	XL16	V1 output
000017A8	00000000 00000000						
000017B0	00000000 00000000			997+	DS	2FD	gap
000017B8	00000000 00000000						
				998+*			
000017C0				999+X9	DS	0F	
000017C0	E310 5024 0014		00000024	1000+	LGF	R1, V2ADDR	load v2 source
000017C6	E761 0000 0806		00000000	1001+	VL	v22, 0(R1)	use v21 to test decoder
000017CC	E310 5028 0014		00000028	1002+	LGF	R1, V3ADDR	load v3 source
000017D2	E771 0000 0806		00000000	1003+	VL	v23, 0(R1)	use v22 to test decoder
000017D8	E756 7010 3E95			1004+	VPKLS	V21, V22, V23, 3, 1	test instruction
000017DE	B98D 0020			1005+	EPSW	R2, R0	extract psw
000017E2	5020 500C		0000000C	1006+	ST	R2, CCPSW	to save CC
000017E6	E750 5048 080E		000017A0	1007+	VST	V21, V109	save v1 output
000017EC	07FB			1008+	BR	R11	return
000017F0				1009+RE9	DC	0F	V1 for this test
000017F0				1010+	DROP	R5	
000017F0	FFFFFFFF FFFFFFFF			1011	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000017F8	FFFFFFFF FFFFFFFF						
00001800	FFFFFFFF FFFFFFFF			1012	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00001808	FFFFFFFF FFFFFFFF						
00001810	FFFFFFFF FFFFFFFF			1013	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00001818	FFFFFFFF FFFFFFFF						
				1014			
				1015	*	-----	
				1016	*	case - general	
				1017	*	-----	
				1018	*	Halfword	
				1019	VRR_B	VPKLS, 1, 0	
00001820				1020+	DS	0FD	
00001820		00001820		1021+	USING	*, R5	base for test data and test routine
00001820	00001888			1022+T10	DC	A(X10)	address of test routine
00001824	000A			1023+	DC	H' 10'	test number
00001826	00			1024+	DC	X' 00'	
00001827	01			1025+	DC	HL1' 1'	m4 used
00001828	01			1026+	DC	HL1' 1'	m5 used
00001829	00			1027+	DC	HL1' 0'	CC
0000182A	07			1028+	DC	HL1' 7'	CC failed mask
0000182C	00000000 00000000			1029+	DS	2F	extracted PSW after test (has CC)
00001834	FF			1030+	DC	X' FF'	extracted CC, if test failed
00001835	E5D7D2D3 E2404040			1031+	DC	CL8' VPKLS'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001840	000018B8			1032+	DC	A(RE10)	address of v1 result
00001844	000018C8			1033+	DC	A(RE10+16)	address of v2 source
00001848	000018D8			1034+	DC	A(RE10+32)	address of v3 source
0000184C	00000010			1035+	DC	A(16)	result length
00001850	000018B8			1036+REA10	DC	A(RE10)	result address
00001858	00000000 00000000			1037+	DS	2FD	gap
00001860	00000000 00000000						
00001868	00000000 00000000			1038+V1010	DS	XL16	V1 output
00001870	00000000 00000000						
00001878	00000000 00000000			1039+	DS	2FD	gap
00001880	00000000 00000000						
00001888				1040+*			
00001888	E310 5024 0014		00000024	1041+X10	DS	0F	
0000188E	E761 0000 0806		00000000	1042+	LGF	R1, V2ADDR	load v2 source
00001894	E310 5028 0014		00000028	1043+	VL	v22, 0(R1)	use v21 to test decoder
0000189A	E771 0000 0806		00000000	1044+	LGF	R1, V3ADDR	load v3 source
000018A0	E756 7010 1E95			1045+	VL	v23, 0(R1)	use v22 to test decoder
000018A6	B98D 0020			1046+	VPKLS	V21, V22, V23, 1, 1	test instruction
000018AA	5020 500C		0000000C	1047+	EPSW	R2, R0	extract psw
000018AE	E750 5048 080E		00001868	1048+	ST	R2, CCPSW	to save CC
000018B4	07FB			1049+	VST	V21, V1010	save v1 output
000018B8				1050+	BR	R11	return
000018B8				1051+RE10	DC	0F	V1 for this test
000018B8				1052+	DROP	R5	
000018B8	11335577 99BBDDFF			1053	DC	XL16' 1133557799BBDDFF FEFDFCFBFAF9F8F7'	result
000018C0	FEFDFCFB FAF9F8F7						
000018C8	00110033 00550077			1054	DC	XL16' 0011003300550077 009900BB00DD00FF'	v2
000018D0	009900BB 00DD00FF						
000018D8	00FE00FD 00FC00FB			1055	DC	XL16' 00FE00FD00FC00FB 00FA00F900F800F7'	v3
000018E0	00FA00F9 00F800F7						
000018E8				1056			
000018E8		000018E8		1057	VRR_B	VPKLS, 1, 0	
000018E8	00001950			1058+	DS	0FD	
000018EC	000B			1059+	USING	*, R5	base for test data and test routine
000018EE	00			1060+T11	DC	A(X11)	address of test routine
000018EF	01			1061+	DC	H' 11'	test number
000018F0	01			1062+	DC	X' 00'	
000018F1	00			1063+	DC	HL1' 1'	m4 used
000018F2	07			1064+	DC	HL1' 1'	m5 used
000018F4	00000000 00000000			1065+	DC	HL1' 0'	CC
000018FC	FF			1066+	DC	HL1' 7'	CC failed mask
000018FD	E5D7D2D3 E2404040			1067+	DS	2F	extracted PSW after test (has CC)
00001908	00001980			1068+	DC	X' FF'	extracted CC, if test failed
0000190C	00001990			1069+	DC	CL8' VPKLS'	instruction name
00001910	000019A0			1070+	DC	A(RE11)	address of v1 result
00001914	00000010			1071+	DC	A(RE11+16)	address of v2 source
00001918	00001980			1072+	DC	A(RE11+32)	address of v3 source
00001920	00000000 00000000			1073+	DC	A(16)	result length
00001928	00000000 00000000			1074+REA11	DC	A(RE11)	result address
00001930	00000000 00000000			1075+	DS	2FD	gap
00001938	00000000 00000000						
00001940	00000000 00000000			1076+V1011	DS	XL16	V1 output
00001948	00000000 00000000						
				1077+	DS	2FD	gap
				1078+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001950				1079+X11	DS	0F	
00001950	E310 5024 0014		00000024	1080+	LGF	R1, V2ADDR	load v2 source
00001956	E761 0000 0806		00000000	1081+	VL	v22, 0(R1)	use v21 to test decoder
0000195C	E310 5028 0014		00000028	1082+	LGF	R1, V3ADDR	load v3 source
00001962	E771 0000 0806		00000000	1083+	VL	v23, 0(R1)	use v22 to test decoder
00001968	E756 7010 1E95			1084+	VPKLS	V21, V22, V23, 1, 1	test instruction
0000196E	B98D 0020			1085+	EPSW	R2, R0	extract psw
00001972	5020 500C		0000000C	1086+	ST	R2, CCPSW	to save CC
00001976	E750 5048 080E		00001930	1087+	VST	V21, V1011	save v1 output
0000197C	07FB			1088+	BR	R11	return
00001980				1089+RE11	DC	0F	V1 for this test
00001980				1090+	DROP	R5	
00001980	FEFDFCFB FAF9F8F7			1091	DC	XL16' FEFDFCFBFAF9F8F7 1133557799BBDDFF'	result
00001988	11335577 99BBDDFF						
00001990	00FE00FD 00FC00FB			1092	DC	XL16' 00FE00FD00FC00FB 00FA00F900F800F7'	v2
00001998	00FA00F9 00F800F7						
000019A0	00110033 00550077			1093	DC	XL16' 0011003300550077 009900BB00DD00FF'	v3
000019A8	009900BB 00DD00FF						
				1094			
				1095	VRR_B	VPKLS, 1, 1	
000019B0				1096+	DS	0FD	
000019B0		000019B0		1097+	USING	*, R5	base for test data and test routine
000019B0	00001A18			1098+T12	DC	A(X12)	address of test routine
000019B4	000C			1099+	DC	H' 12'	test number
000019B6	00			1100+	DC	X' 00'	
000019B7	01			1101+	DC	HL1' 1'	m4 used
000019B8	01			1102+	DC	HL1' 1'	m5 used
000019B9	01			1103+	DC	HL1' 1'	CC
000019BA	0B			1104+	DC	HL1' 11'	CC failed mask
000019BC	00000000 00000000			1105+	DS	2F	extracted PSW after test (has CC)
000019C4	FF			1106+	DC	X' FF'	extracted CC, if test failed
000019C5	E5D7D2D3 E2404040			1107+	DC	CL8' VPKLS'	instruction name
000019D0	00001A48			1108+	DC	A(RE12)	address of v1 result
000019D4	00001A58			1109+	DC	A(RE12+16)	address of v2 source
000019D8	00001A68			1110+	DC	A(RE12+32)	address of v3 source
000019DC	00000010			1111+	DC	A(16)	result length
000019E0	00001A48			1112+REA12	DC	A(RE12)	result address
000019E8	00000000 00000000			1113+	DS	2FD	gap
000019F0	00000000 00000000						
000019F8	00000000 00000000			1114+V1012	DS	XL16	V1 output
00001A00	00000000 00000000						
00001A08	00000000 00000000			1115+	DS	2FD	gap
00001A10	00000000 00000000						
				1116+*			
00001A18				1117+X12	DS	0F	
00001A18	E310 5024 0014		00000024	1118+	LGF	R1, V2ADDR	load v2 source
00001A1E	E761 0000 0806		00000000	1119+	VL	v22, 0(R1)	use v21 to test decoder
00001A24	E310 5028 0014		00000028	1120+	LGF	R1, V3ADDR	load v3 source
00001A2A	E771 0000 0806		00000000	1121+	VL	v23, 0(R1)	use v22 to test decoder
00001A30	E756 7010 1E95			1122+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001A36	B98D 0020			1123+	EPSW	R2, R0	extract psw
00001A3A	5020 500C		0000000C	1124+	ST	R2, CCPSW	to save CC
00001A3E	E750 5048 080E		000019F8	1125+	VST	V21, V1012	save v1 output
00001A44	07FB			1126+	BR	R11	return
00001A48				1127+RE12	DC	0F	V1 for this test
00001A48				1128+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001A48	01FFFFFF FFFFFFFF			1129	DC	XL16' 01FFFFFFF000000000 1133557799BBDDFF'	result
00001A50	11335577 99BBDDFF						
00001A58	00010203 04050607			1130	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001A60	08090A0B 0C0D0E0F						
00001A68	00110033 00550077			1131	DC	XL16' 0011003300550077 009900BB00DD00FF'	v3
00001A70	009900BB 00DD00FF						
				1132			
				1133	VRR_B	VPKLS, 1, 1	
00001A78				1134+	DS	0FD	
00001A78		00001A78		1135+	USING	*, R5	base for test data and test routine
00001A78	00001AE0			1136+T13	DC	A(X13)	address of test routine
00001A7C	000D			1137+	DC	H' 13'	test number
00001A7E	00			1138+	DC	X' 00'	
00001A7F	01			1139+	DC	HL1' 1'	m4 used
00001A80	01			1140+	DC	HL1' 1'	m5 used
00001A81	01			1141+	DC	HL1' 1'	CC
00001A82	0B			1142+	DC	HL1' 11'	CC failed mask
00001A84	00000000 00000000			1143+	DS	2F	extracted PSW after test (has CC)
00001A8C	FF			1144+	DC	X' FF'	extracted CC, if test failed
00001A8D	E5D7D2D3 E2404040			1145+	DC	CL8' VPKLS'	instruction name
00001A98	00001B10			1146+	DC	A(RE13)	address of v1 result
00001A9C	00001B20			1147+	DC	A(RE13+16)	address of v2 source
00001AA0	00001B30			1148+	DC	A(RE13+32)	address of v3 source
00001AA4	00000010			1149+	DC	A(16)	result length
00001AA8	00001B10			1150+REA13	DC	A(RE13)	result address
00001AB0	00000000 00000000			1151+	DS	2FD	gap
00001AB8	00000000 00000000						
00001AC0	00000000 00000000			1152+V1013	DS	XL16	V1 output
00001AC8	00000000 00000000						
00001AD0	00000000 00000000			1153+	DS	2FD	gap
00001AD8	00000000 00000000						
				1154+*			
00001AE0				1155+X13	DS	0F	
00001AE0	E310 5024 0014		00000024	1156+	LGF	R1, V2ADDR	load v2 source
00001AE6	E761 0000 0806		00000000	1157+	VL	v22, 0(R1)	use v21 to test decoder
00001AEC	E310 5028 0014		00000028	1158+	LGF	R1, V3ADDR	load v3 source
00001AF2	E771 0000 0806		00000000	1159+	VL	v23, 0(R1)	use v22 to test decoder
00001AF8	E756 7010 1E95			1160+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001AFE	B98D 0020			1161+	EPSW	R2, R0	extract psw
00001B02	5020 500C		0000000C	1162+	ST	R2, CCPSW	to save CC
00001B06	E750 5048 080E		00001AC0	1163+	VST	V21, V1013	save v1 output
00001B0C	07FB			1164+	BR	R11	return
00001B10				1165+RE13	DC	0F	V1 for this test
00001B10				1166+	DROP	R5	
00001B10	11335577 99BBDDFF			1167	DC	XL16' 1133557799BBDDFF 01FFFFFFF000000000'	result
00001B18	01FFFFFF FFFFFFFF						
00001B20	00110033 00550077			1168	DC	XL16' 0011003300550077 009900BB00DD00FF'	v2
00001B28	009900BB 00DD00FF						
00001B30	00010203 04050607			1169	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00001B38	08090A0B 0C0D0E0F						
				1170			
				1171	VRR_B	VPKLS, 1, 3	
00001B40				1172+	DS	0FD	
00001B40		00001B40		1173+	USING	*, R5	base for test data and test routine
00001B40	00001BA8			1174+T14	DC	A(X14)	address of test routine
00001B44	000E			1175+	DC	H' 14'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001B46	00			1176+	DC	X' 00'	
00001B47	01			1177+	DC	HL1' 1'	m4 used
00001B48	01			1178+	DC	HL1' 1'	m5 used
00001B49	03			1179+	DC	HL1' 3'	CC
00001B4A	0E			1180+	DC	HL1' 14'	CC failed mask
00001B4C	00000000	00000000		1181+	DS	2F	extracted PSW after test (has CC)
00001B54	FF			1182+	DC	X' FF'	extracted CC, if test failed
00001B55	E5D7D2D3	E2404040		1183+	DC	CL8' VPKLS'	instruction name
00001B60	00001BD8			1184+	DC	A(RE14)	address of v1 result
00001B64	00001BE8			1185+	DC	A(RE14+16)	address of v2 source
00001B68	00001BF8			1186+	DC	A(RE14+32)	address of v3 source
00001B6C	00000010			1187+	DC	A(16)	result length
00001B70	00001BD8			1188+REA14	DC	A(RE14)	result address
00001B78	00000000	00000000		1189+	DS	2FD	gap
00001B80	00000000	00000000					
00001B88	00000000	00000000		1190+V1014	DS	XL16	V1 output
00001B90	00000000	00000000					
00001B98	00000000	00000000		1191+	DS	2FD	gap
00001BA0	00000000	00000000					
				1192+*			
00001BA8				1193+X14	DS	0F	
00001BA8	E310 5024 0014		00000024	1194+	LGF	R1, V2ADDR	load v2 source
00001BAE	E761 0000 0806		00000000	1195+	VL	v22, 0(R1)	use v21 to test decoder
00001BB4	E310 5028 0014		00000028	1196+	LGF	R1, V3ADDR	load v3 source
00001BBA	E771 0000 0806		00000000	1197+	VL	v23, 0(R1)	use v22 to test decoder
00001BC0	E756 7010 1E95			1198+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001BC6	B98D 0020			1199+	EPSW	R2, R0	extract psw
00001BCA	5020 500C		0000000C	1200+	ST	R2, CCPSW	to save CC
00001BCE	E750 5048 080E		00001B88	1201+	VST	V21, V1014	save v1 output
00001BD4	07FB			1202+	BR	R11	return
00001BD8				1203+RE14	DC	0F	V1 for this test
00001BD8				1204+	DROP	R5	
00001BD8	FFFFFFFF	FFFFFFFF		1205	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00001BE0	FFFFFFFF	FFFFFFFF					
00001BE8	01110133	01550177		1206	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00001BF0	019901BB	01DD01FF					
00001BF8	01010203	04050607		1207	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00001C00	08090A0B	0C0D0E0F					
				1208			
				1209	VRR_B	VPKLS, 1, 3	
00001C08				1210+	DS	0FD	
00001C08		00001C08		1211+	USING	*, R5	base for test data and test routine
00001C08	00001C70			1212+T15	DC	A(X15)	address of test routine
00001C0C	000F			1213+	DC	H' 15'	test number
00001C0E	00			1214+	DC	X' 00'	
00001C0F	01			1215+	DC	HL1' 1'	m4 used
00001C10	01			1216+	DC	HL1' 1'	m5 used
00001C11	03			1217+	DC	HL1' 3'	CC
00001C12	0E			1218+	DC	HL1' 14'	CC failed mask
00001C14	00000000	00000000		1219+	DS	2F	extracted PSW after test (has CC)
00001C1C	FF			1220+	DC	X' FF'	extracted CC, if test failed
00001C1D	E5D7D2D3	E2404040		1221+	DC	CL8' VPKLS'	instruction name
00001C28	00001CA0			1222+	DC	A(RE15)	address of v1 result
00001C2C	00001CB0			1223+	DC	A(RE15+16)	address of v2 source
00001C30	00001CC0			1224+	DC	A(RE15+32)	address of v3 source
00001C34	00000010			1225+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001C38	00001CA0			1226+REA15	DC	A(RE15)	result address
00001C40	00000000 00000000			1227+	DS	2FD	gap
00001C48	00000000 00000000						
00001C50	00000000 00000000			1228+V1015	DS	XL16	V1 output
00001C58	00000000 00000000						
00001C60	00000000 00000000			1229+	DS	2FD	gap
00001C68	00000000 00000000						
				1230+*			
00001C70				1231+X15	DS	0F	
00001C70	E310 5024 0014		00000024	1232+	LGF	R1, V2ADDR	load v2 source
00001C76	E761 0000 0806		00000000	1233+	VL	v22, 0(R1)	use v21 to test decoder
00001C7C	E310 5028 0014		00000028	1234+	LGF	R1, V3ADDR	load v3 source
00001C82	E771 0000 0806		00000000	1235+	VL	v23, 0(R1)	use v22 to test decoder
00001C88	E756 7010 1E95			1236+	VPKLS	V21, V22, V23, 1, 1	test instruction
00001C8E	B98D 0020			1237+	EPSW	R2, R0	extract psw
00001C92	5020 500C		0000000C	1238+	ST	R2, CCPSW	to save CC
00001C96	E750 5048 080E		00001C50	1239+	VST	V21, V1015	save v1 output
00001C9C	07FB			1240+	BR	R11	return
00001CA0				1241+RE15	DC	0F	V1 for this test
00001CA0				1242+	DROP	R5	
00001CA0	FFFFFFFF FFFFFFFF			1243	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00001CA8	FFFFFFFF FFFFFFFF						
00001CB0	01010203 04050607			1244	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00001CB8	08090A0B 0C0D0E0F						
00001CC0	01110133 01550177			1245	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00001CC8	019901BB 01DD01FF						
				1246			
				1247 *Word			
				1248	VRR_B	VPKLS, 2, 0	
00001CD0				1249+	DS	0FD	
00001CD0		00001CD0		1250+	USING	*, R5	base for test data and test routine
00001CD0	00001D38			1251+T16	DC	A(X16)	address of test routine
00001CD4	0010			1252+	DC	H' 16'	test number
00001CD6	00			1253+	DC	X' 00'	
00001CD7	02			1254+	DC	HL1' 2'	m4 used
00001CD8	01			1255+	DC	HL1' 1'	m5 used
00001CD9	00			1256+	DC	HL1' 0'	CC
00001CDA	07			1257+	DC	HL1' 7'	CC failed mask
00001CDC	00000000 00000000			1258+	DS	2F	extracted PSW after test (has CC)
00001CE4	FF			1259+	DC	X' FF'	extracted CC, if test failed
00001CE5	E5D7D2D3 E2404040			1260+	DC	CL8' VPKLS'	instruction name
00001CF0	00001D68			1261+	DC	A(RE16)	address of v1 result
00001CF4	00001D78			1262+	DC	A(RE16+16)	address of v2 source
00001CF8	00001D88			1263+	DC	A(RE16+32)	address of v3 source
00001CFC	00000010			1264+	DC	A(16)	result length
00001D00	00001D68			1265+REA16	DC	A(RE16)	result address
00001D08	00000000 00000000			1266+	DS	2FD	gap
00001D10	00000000 00000000						
00001D18	00000000 00000000			1267+V1016	DS	XL16	V1 output
00001D20	00000000 00000000						
00001D28	00000000 00000000			1268+	DS	2FD	gap
00001D30	00000000 00000000						
				1269+*			
00001D38				1270+X16	DS	0F	
00001D38	E310 5024 0014		00000024	1271+	LGF	R1, V2ADDR	load v2 source
00001D3E	E761 0000 0806		00000000	1272+	VL	v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001D44	E310 5028 0014		00000028	1273+	LGF	R1, V3ADDR	load v3 source
00001D4A	E771 0000 0806		00000000	1274+	VL	v23, 0(R1)	use v22 to test decoder
00001D50	E756 7010 2E95			1275+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001D56	B98D 0020			1276+	EPSW	R2, R0	extract psw
00001D5A	5020 500C		0000000C	1277+	ST	R2, CCPSW	to save CC
00001D5E	E750 5048 080E		00001D18	1278+	VST	V21, V1016	save v1 output
00001D64	07FB			1279+	BR	R11	return
00001D68				1280+RE16	DC	0F	V1 for this test
00001D68				1281+	DROP	R5	
00001D68	11335577 99BBDDFF			1282	DC	XL16' 1133557799BBDDFF FEFDFCFBFAF9F8F7'	result t
00001D70	FEFDFCFB FAF9F8F7						
00001D78	00001133 00005577			1283	DC	XL16' 0000113300005577 000099BB0000DDFF'	v2
00001D80	000099BB 0000DDFF						
00001D88	0000FEFD 0000FCFB			1284	DC	XL16' 0000FEFD0000FCFB 0000FAF90000F8F7'	v3
00001D90	0000FAF9 0000F8F7						
				1285			
				1286	VRR_B	VPKLS, 2, 0	
00001D98				1287+	DS	0FD	
00001D98		00001D98		1288+	USING	*, R5	base for test data and test routine
00001D98	00001E00			1289+T17	DC	A(X17)	address of test routine
00001D9C	0011			1290+	DC	H' 17'	test number
00001D9E	00			1291+	DC	X' 00'	
00001D9F	02			1292+	DC	HL1' 2'	m4 used
00001DA0	01			1293+	DC	HL1' 1'	m5 used
00001DA1	00			1294+	DC	HL1' 0'	CC
00001DA2	07			1295+	DC	HL1' 7'	CC failed mask
00001DA4	00000000 00000000			1296+	DS	2F	extracted PSW after test (has CC)
00001DAC	FF			1297+	DC	X' FF'	extracted CC, if test failed
00001DAD	E5D7D2D3 E2404040			1298+	DC	CL8' VPKLS'	instruction name
00001DB8	00001E30			1299+	DC	A(RE17)	address of v1 result
00001DBC	00001E40			1300+	DC	A(RE17+16)	address of v2 source
00001DC0	00001E50			1301+	DC	A(RE17+32)	address of v3 source
00001DC4	00000010			1302+	DC	A(16)	result length
00001DC8	00001E30			1303+REA17	DC	A(RE17)	result address
00001DD0	00000000 00000000			1304+	DS	2FD	gap
00001DD8	00000000 00000000						
00001DE0	00000000 00000000			1305+V1017	DS	XL16	V1 output
00001DE8	00000000 00000000						
00001DF0	00000000 00000000			1306+	DS	2FD	gap
00001DF8	00000000 00000000						
				1307+*			
00001E00				1308+X17	DS	0F	
00001E00	E310 5024 0014		00000024	1309+	LGF	R1, V2ADDR	load v2 source
00001E06	E761 0000 0806		00000000	1310+	VL	v22, 0(R1)	use v21 to test decoder
00001E0C	E310 5028 0014		00000028	1311+	LGF	R1, V3ADDR	load v3 source
00001E12	E771 0000 0806		00000000	1312+	VL	v23, 0(R1)	use v22 to test decoder
00001E18	E756 7010 2E95			1313+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001E1E	B98D 0020			1314+	EPSW	R2, R0	extract psw
00001E22	5020 500C		0000000C	1315+	ST	R2, CCPSW	to save CC
00001E26	E750 5048 080E		00001DE0	1316+	VST	V21, V1017	save v1 output
00001E2C	07FB			1317+	BR	R11	return
00001E30				1318+RE17	DC	0F	V1 for this test
00001E30				1319+	DROP	R5	
00001E30	FEFDFCFB FAF9F8F7			1320	DC	XL16' FEFDFCFBFAF9F8F7 1133557799BBDDFF'	result t
00001E38	11335577 99BBDDFF						
00001E40	0000FEFD 0000FCFB			1321	DC	XL16' 0000FEFD0000FCFB 0000FAF90000F8F7'	v2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001E48	0000FAF9	0000F8F7						
00001E50	00001133	00005577		1322	DC	XL16'	0000113300005577 000099BB0000DDFF'	v3
00001E58	000099BB	0000DDFF						
				1323				
				1324	VRR_B	VPKLS, 2, 1		
00001E60				1325+	DS	0FD		
00001E60		00001E60		1326+	USING	*, R5	base for test data and test routine	
00001E60	00001EC8			1327+T18	DC	A(X18)	address of test routine	
00001E64	0012			1328+	DC	H' 18'	test number	
00001E66	00			1329+	DC	X' 00'		
00001E67	02			1330+	DC	HL1' 2'	m4 used	
00001E68	01			1331+	DC	HL1' 1'	m5 used	
00001E69	01			1332+	DC	HL1' 1'	CC	
00001E6A	0B			1333+	DC	HL1' 11'	CC failed mask	
00001E6C	00000000	00000000		1334+	DS	2F	extracted PSW after test (has CC)	
00001E74	FF			1335+	DC	X' FF'	extracted CC, if test failed	
00001E75	E5D7D2D3	E2404040		1336+	DC	CL8' VPKLS'	instruction name	
00001E80	00001EF8			1337+	DC	A(RE18)	address of v1 result	
00001E84	00001F08			1338+	DC	A(RE18+16)	address of v2 source	
00001E88	00001F18			1339+	DC	A(RE18+32)	address of v3 source	
00001E8C	00000010			1340+	DC	A(16)	result length	
00001E90	00001EF8			1341+REA18	DC	A(RE18)	result address	
00001E98	00000000	00000000		1342+	DS	2FD	gap	
00001EA0	00000000	00000000						
00001EA8	00000000	00000000		1343+V1018	DS	XL16	V1 output	
00001EB0	00000000	00000000						
00001EB8	00000000	00000000		1344+	DS	2FD	gap	
00001EC0	00000000	00000000						
				1345+*				
00001EC8				1346+X18	DS	0F		
00001EC8	E310 5024 0014		00000024	1347+	LGF	R1, V2ADDR	load v2 source	
00001ECE	E761 0000 0806		00000000	1348+	VL	v22, 0(R1)	use v21 to test decoder	
00001ED4	E310 5028 0014		00000028	1349+	LGF	R1, V3ADDR	load v3 source	
00001EDA	E771 0000 0806		00000000	1350+	VL	v23, 0(R1)	use v22 to test decoder	
00001EE0	E756 7010 2E95			1351+	VPKLS	V21, V22, V23, 2, 1	test instruction	
00001EE6	B98D 0020			1352+	EPSW	R2, R0	extract psw	
00001EEA	5020 500C		0000000C	1353+	ST	R2, CCPSW	to save CC	
00001EEE	E750 5048 080E		00001EA8	1354+	VST	V21, V1018	save v1 output	
00001EF4	07FB			1355+	BR	R11	return	
00001EF8				1356+RE18	DC	0F	V1 for this test	
00001EF8				1357+	DROP	R5		
00001EF8	1203FFFF	FFFFFFFF		1358	DC	XL16' 1203FFFFFFFFFFFFFFFF 1133557799BBDDFF'	result t	
00001F00	11335577	99BBDDFF						
00001F08	00001203	04050607		1359	DC	XL16' 0000120304050607 08090A0B0C0D0E0F'	v2	
00001F10	08090A0B	0C0D0E0F						
00001F18	00001133	00005577		1360	DC	XL16' 0000113300005577 000099BB0000DDFF'	v3	
00001F20	000099BB	0000DDFF						
				1361				
				1362	VRR_B	VPKLS, 2, 1		
00001F28				1363+	DS	0FD		
00001F28		00001F28		1364+	USING	*, R5	base for test data and test routine	
00001F28	00001F90			1365+T19	DC	A(X19)	address of test routine	
00001F2C	0013			1366+	DC	H' 19'	test number	
00001F2E	00			1367+	DC	X' 00'		
00001F2F	02			1368+	DC	HL1' 2'	m4 used	
00001F30	01			1369+	DC	HL1' 1'	m5 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001F31	01			1370+	DC	HL1' 1'	CC
00001F32	0B			1371+	DC	HL1' 11'	CC failed mask
00001F34	00000000 00000000			1372+	DS	2F	extracted PSW after test (has CC)
00001F3C	FF			1373+	DC	X' FF'	extracted CC, if test failed
00001F3D	E5D7D2D3 E2404040			1374+	DC	CL8' VPKLS'	instruction name
00001F48	00001FC0			1375+	DC	A(RE19)	address of v1 result
00001F4C	00001FD0			1376+	DC	A(RE19+16)	address of v2 source
00001F50	00001FE0			1377+	DC	A(RE19+32)	address of v3 source
00001F54	00000010			1378+	DC	A(16)	result length
00001F58	00001FC0			1379+REA19	DC	A(RE19)	result address
00001F60	00000000 00000000			1380+	DS	2FD	gap
00001F68	00000000 00000000						
00001F70	00000000 00000000			1381+V1019	DS	XL16	V1 output
00001F78	00000000 00000000						
00001F80	00000000 00000000			1382+	DS	2FD	gap
00001F88	00000000 00000000						
				1383+*			
00001F90				1384+X19	DS	0F	
00001F90	E310 5024 0014		00000024	1385+	LGF	R1, V2ADDR	load v2 source
00001F96	E761 0000 0806		00000000	1386+	VL	v22, 0(R1)	use v21 to test decoder
00001F9C	E310 5028 0014		00000028	1387+	LGF	R1, V3ADDR	load v3 source
00001FA2	E771 0000 0806		00000000	1388+	VL	v23, 0(R1)	use v22 to test decoder
00001FA8	E756 7010 2E95			1389+	VPKLS	V21, V22, V23, 2, 1	test instruction
00001FAE	B98D 0020			1390+	EPSW	R2, R0	extract psw
00001FB2	5020 500C		0000000C	1391+	ST	R2, CCPSW	to save CC
00001FB6	E750 5048 080E		00001F70	1392+	VST	V21, V1019	save v1 output
00001FBC	07FB			1393+	BR	R11	return
00001FC0				1394+RE19	DC	0F	V1 for this test
00001FC0				1395+	DROP	R5	
00001FC0	11335577 99BBDDFF			1396	DC	XL16' 1133557799BBDDFF 1203FFFFFFFFFFFFFF'	result
00001FC8	1203FFFF FFFFFFFF						
00001FD0	00001133 00005577			1397	DC	XL16' 0000113300005577 000099BB0000DDFF'	v2
00001FD8	000099BB 0000DDFF						
00001FE0	00001203 04050607			1398	DC	XL16' 0000120304050607 08090A0B0C0D0E0F'	v3
00001FE8	08090A0B 0C0D0E0F						
				1399			
00001FF0				1400	VRR_B	VPKLS, 2, 3	
00001FF0		00001FF0		1401+	DS	0FD	
00001FF0	00002058			1402+	USING	*, R5	base for test data and test routine
00001FF4	0014			1403+T20	DC	A(X20)	address of test routine
00001FF6	00			1404+	DC	H' 20'	test number
00001FF7	02			1405+	DC	X' 00'	
00001FF8	01			1406+	DC	HL1' 2'	m4 used
00001FF9	03			1407+	DC	HL1' 1'	m5 used
00001FFA	0E			1408+	DC	HL1' 3'	CC
00001FFC	00000000 00000000			1409+	DC	HL1' 14'	CC failed mask
00002004	FF			1410+	DS	2F	extracted PSW after test (has CC)
00002005	E5D7D2D3 E2404040			1411+	DC	X' FF'	extracted CC, if test failed
00002010	00002088			1412+	DC	CL8' VPKLS'	instruction name
00002014	00002098			1413+	DC	A(RE20)	address of v1 result
00002018	000020A8			1414+	DC	A(RE20+16)	address of v2 source
0000201C	00000010			1415+	DC	A(RE20+32)	address of v3 source
00002020	00002088			1416+	DC	A(16)	result length
00002028	00000000 00000000			1417+REA20	DC	A(RE20)	result address
00002030	00000000 00000000			1418+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002038	00000000 00000000			1419+V1020	DS	XL16	V1 output
00002040	00000000 00000000						
00002048	00000000 00000000			1420+	DS	2FD	gap
00002050	00000000 00000000						
				1421+*			
00002058				1422+X20	DS	0F	
00002058	E310 5024 0014		00000024	1423+	LGF	R1, V2ADDR	load v2 source
0000205E	E761 0000 0806		00000000	1424+	VL	v22, 0(R1)	use v21 to test decoder
00002064	E310 5028 0014		00000028	1425+	LGF	R1, V3ADDR	load v3 source
0000206A	E771 0000 0806		00000000	1426+	VL	v23, 0(R1)	use v22 to test decoder
00002070	E756 7010 2E95			1427+	VPKLS	V21, V22, V23, 2, 1	test instruction
00002076	B98D 0020			1428+	EPSW	R2, R0	extract psw
0000207A	5020 500C		0000000C	1429+	ST	R2, CCPSW	to save CC
0000207E	E750 5048 080E		00002038	1430+	VST	V21, V1020	save v1 output
00002084	07FB			1431+	BR	R11	return
00002088				1432+RE20	DC	0F	V1 for this test
00002088				1433+	DROP	R5	
00002088	FFFFFFFF FFFFFFFF			1434	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00002090	FFFFFFFF FFFFFFFF						
00002098	01110133 01550177			1435	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
000020A0	019901BB 01DD01FF						
000020A8	01010203 04050607			1436	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
000020B0	08090A0B 0C0D0E0F						
				1437			
				1438	VRR_B	VPKLS, 2, 3	
000020B8				1439+	DS	0FD	
000020B8		000020B8		1440+	USING	*, R5	base for test data and test routine
000020B8	00002120			1441+T21	DC	A(X21)	address of test routine
000020BC	0015			1442+	DC	H' 21'	test number
000020BE	00			1443+	DC	X' 00'	
000020BF	02			1444+	DC	HL1' 2'	m4 used
000020C0	01			1445+	DC	HL1' 1'	m5 used
000020C1	03			1446+	DC	HL1' 3'	CC
000020C2	0E			1447+	DC	HL1' 14'	CC failed mask
000020C4	00000000 00000000			1448+	DS	2F	extracted PSW after test (has CC)
000020CC	FF			1449+	DC	X' FF'	extracted CC, if test failed
000020CD	E5D7D2D3 E2404040			1450+	DC	CL8' VPKLS'	instruction name
000020D8	00002150			1451+	DC	A(RE21)	address of v1 result
000020DC	00002160			1452+	DC	A(RE21+16)	address of v2 source
000020E0	00002170			1453+	DC	A(RE21+32)	address of v3 source
000020E4	00000010			1454+	DC	A(16)	result length
000020E8	00002150			1455+REA21	DC	A(RE21)	result address
000020F0	00000000 00000000			1456+	DS	2FD	gap
000020F8	00000000 00000000						
00002100	00000000 00000000			1457+V1021	DS	XL16	V1 output
00002108	00000000 00000000						
00002110	00000000 00000000			1458+	DS	2FD	gap
00002118	00000000 00000000						
				1459+*			
00002120				1460+X21	DS	0F	
00002120	E310 5024 0014		00000024	1461+	LGF	R1, V2ADDR	load v2 source
00002126	E761 0000 0806		00000000	1462+	VL	v22, 0(R1)	use v21 to test decoder
0000212C	E310 5028 0014		00000028	1463+	LGF	R1, V3ADDR	load v3 source
00002132	E771 0000 0806		00000000	1464+	VL	v23, 0(R1)	use v22 to test decoder
00002138	E756 7010 2E95			1465+	VPKLS	V21, V22, V23, 2, 1	test instruction
0000213E	B98D 0020			1466+	EPSW	R2, R0	extract psw

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002142	5020 500C		0000000C	1467+	ST	R2, CCPSW	to save CC	
00002146	E750 5048 080E		00002100	1468+	VST	V21, V1021	save v1 output	
0000214C	07FB			1469+	BR	R11	return	
00002150				1470+RE21	DC	0F	V1 for this test	
00002150				1471+	DROP	R5		
00002150	FFFFFFFF FFFFFFFF			1472	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00002158	FFFFFFFF FFFFFFFF							
00002160	01010203 04050607			1473	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2	
00002168	08090A0B 0C0D0E0F							
00002170	01110133 01550177			1474	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3	
00002178	019901BB 01DD01FF							
				1475				
				1476 *Doubleword				
				1477	VRR_B	VPKLS, 3, 0		
00002180				1478+	DS	0FD		
00002180		00002180		1479+	USING	*, R5	base for test data and test routine	
00002180	000021E8			1480+T22	DC	A(X22)	address of test routine	
00002184	0016			1481+	DC	H' 22'	test number	
00002186	00			1482+	DC	X' 00'		
00002187	03			1483+	DC	HL1' 3'	m4 used	
00002188	01			1484+	DC	HL1' 1'	m5 used	
00002189	00			1485+	DC	HL1' 0'	CC	
0000218A	07			1486+	DC	HL1' 7'	CC failed mask	
0000218C	00000000 00000000			1487+	DS	2F	extracted PSW after test (has CC)	
00002194	FF			1488+	DC	X' FF'	extracted CC, if test failed	
00002195	E5D7D2D3 E2404040			1489+	DC	CL8' VPKLS'	instruction name	
000021A0	00002218			1490+	DC	A(RE22)	address of v1 result	
000021A4	00002228			1491+	DC	A(RE22+16)	address of v2 source	
000021A8	00002238			1492+	DC	A(RE22+32)	address of v3 source	
000021AC	00000010			1493+	DC	A(16)	result length	
000021B0	00002218			1494+REA22	DC	A(RE22)	result address	
000021B8	00000000 00000000			1495+	DS	2FD	gap	
000021C0	00000000 00000000							
000021C8	00000000 00000000			1496+V1022	DS	XL16	V1 output	
000021D0	00000000 00000000							
000021D8	00000000 00000000			1497+	DS	2FD	gap	
000021E0	00000000 00000000							
				1498+*				
000021E8				1499+X22	DS	0F		
000021E8	E310 5024 0014		00000024	1500+	LGF	R1, V2ADDR	load v2 source	
000021EE	E761 0000 0806		00000000	1501+	VL	v22, 0(R1)	use v21 to test decoder	
000021F4	E310 5028 0014		00000028	1502+	LGF	R1, V3ADDR	load v3 source	
000021FA	E771 0000 0806		00000000	1503+	VL	v23, 0(R1)	use v22 to test decoder	
00002200	E756 7010 3E95			1504+	VPKLS	V21, V22, V23, 3, 1	test instruction	
00002206	B98D 0020			1505+	EPSW	R2, R0	extract psw	
0000220A	5020 500C		0000000C	1506+	ST	R2, CCPSW	to save CC	
0000220E	E750 5048 080E		000021C8	1507+	VST	V21, V1022	save v1 output	
00002214	07FB			1508+	BR	R11	return	
00002218				1509+RE22	DC	0F	V1 for this test	
00002218				1510+	DROP	R5		
00002218	11335577 99BBDDFF			1511	DC	XL16' 1133557799BBDDFF FEFDFCFBFAF9F8F7'	result t	
00002220	FEFDFCFB FAF9F8F7							
00002228	00000000 11335577			1512	DC	XL16' 0000000011335577 0000000099BBDDFF'	v2	
00002230	00000000 99BBDDFF							
00002238	00000000 FEFDFCFB			1513	DC	XL16' 00000000FEFDFCFB 00000000FAF9F8F7'	v3	
00002240	00000000 FAF9F8F7							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1514			
				1515	VRR_B	VPKLS, 3, 0	
00002248				1516+	DS	0FD	
00002248		00002248		1517+	USING	*, R5	base for test data and test routine
00002248	000022B0			1518+T23	DC	A(X23)	address of test routine
0000224C	0017			1519+	DC	H' 23'	test number
0000224E	00			1520+	DC	X' 00'	
0000224F	03			1521+	DC	HL1' 3'	m4 used
00002250	01			1522+	DC	HL1' 1'	m5 used
00002251	00			1523+	DC	HL1' 0'	CC
00002252	07			1524+	DC	HL1' 7'	CC failed mask
00002254	00000000 00000000			1525+	DS	2F	extracted PSW after test (has CC)
0000225C	FF			1526+	DC	X' FF'	extracted CC, if test failed
0000225D	E5D7D2D3 E2404040			1527+	DC	CL8' VPKLS'	instruction name
00002268	000022E0			1528+	DC	A(RE23)	address of v1 result
0000226C	000022F0			1529+	DC	A(RE23+16)	address of v2 source
00002270	00002300			1530+	DC	A(RE23+32)	address of v3 source
00002274	00000010			1531+	DC	A(16)	result length
00002278	000022E0			1532+REA23	DC	A(RE23)	result address
00002280	00000000 00000000			1533+	DS	2FD	gap
00002288	00000000 00000000						
00002290	00000000 00000000			1534+V1023	DS	XL16	V1 output
00002298	00000000 00000000						
000022A0	00000000 00000000			1535+	DS	2FD	gap
000022A8	00000000 00000000						
				1536+*			
000022B0				1537+X23	DS	0F	
000022B0	E310 5024 0014		00000024	1538+	LGF	R1, V2ADDR	load v2 source
000022B6	E761 0000 0806		00000000	1539+	VL	v22, 0(R1)	use v21 to test decoder
000022BC	E310 5028 0014		00000028	1540+	LGF	R1, V3ADDR	load v3 source
000022C2	E771 0000 0806		00000000	1541+	VL	v23, 0(R1)	use v22 to test decoder
000022C8	E756 7010 3E95			1542+	VPKLS	V21, V22, V23, 3, 1	test instruction
000022CE	B98D 0020			1543+	EPSW	R2, R0	extract psw
000022D2	5020 500C		0000000C	1544+	ST	R2, CCPSW	to save CC
000022D6	E750 5048 080E		00002290	1545+	VST	V21, V1023	save v1 output
000022DC	07FB			1546+	BR	R11	return
000022E0				1547+RE23	DC	0F	V1 for this test
000022E0				1548+	DROP	R5	
000022E0	FEFDFCFB FAF9F8F7			1549	DC	XL16' FEFDFCFBFAF9F8F7 1133557799BBDDFF'	result t
000022E8	11335577 99BBDDFF						
000022F0	00000000 FEFDFCFB			1550	DC	XL16' 00000000FEFDFCFB 00000000FAF9F8F7'	v2
000022F8	00000000 FAF9F8F7						
00002300	00000000 11335577			1551	DC	XL16' 0000000011335577 0000000099BBDDFF'	v3
00002308	00000000 99BBDDFF						
				1552			
				1553	VRR_B	VPKLS, 3, 1	
00002310				1554+	DS	0FD	
00002310		00002310		1555+	USING	*, R5	base for test data and test routine
00002310	00002378			1556+T24	DC	A(X24)	address of test routine
00002314	0018			1557+	DC	H' 24'	test number
00002316	00			1558+	DC	X' 00'	
00002317	03			1559+	DC	HL1' 3'	m4 used
00002318	01			1560+	DC	HL1' 1'	m5 used
00002319	01			1561+	DC	HL1' 1'	CC
0000231A	0B			1562+	DC	HL1' 11'	CC failed mask
0000231C	00000000 00000000			1563+	DS	2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002324	FF			1564+	DC	X' FF'	extracted CC, if test failed
00002325	E5D7D2D3 E2404040			1565+	DC	CL8' VPKLS'	instruction name
00002330	000023A8			1566+	DC	A(RE24)	address of v1 result
00002334	000023B8			1567+	DC	A(RE24+16)	address of v2 source
00002338	000023C8			1568+	DC	A(RE24+32)	address of v3 source
0000233C	00000010			1569+	DC	A(16)	result length
00002340	000023A8			1570+REA24	DC	A(RE24)	result address
00002348	00000000 00000000			1571+	DS	2FD	gap
00002350	00000000 00000000						
00002358	00000000 00000000			1572+V1024	DS	XL16	V1 output
00002360	00000000 00000000						
00002368	00000000 00000000			1573+	DS	2FD	gap
00002370	00000000 00000000						
00002378				1574+*			
00002378	E310 5024 0014		00000024	1575+X24	DS	0F	
0000237E	E761 0000 0806		00000000	1576+	LGF	R1, V2ADDR	load v2 source
00002384	E310 5028 0014		00000028	1577+	VL	v22, 0(R1)	use v21 to test decoder
0000238A	E771 0000 0806		00000000	1578+	LGF	R1, V3ADDR	load v3 source
00002390	E756 7010 3E95			1579+	VL	v23, 0(R1)	use v22 to test decoder
00002396	B98D 0020			1580+	VPKLS	V21, V22, V23, 3, 1	test instruction
0000239A	5020 500C		0000000C	1581+	EPSW	R2, R0	extract psw
0000239E	E750 5048 080E		00002358	1582+	ST	R2, CCPSW	to save CC
000023A4	07FB			1583+	VST	V21, V1024	save v1 output
000023A8				1584+	BR	R11	return
000023A8				1585+RE24	DC	0F	V1 for this test
000023A8				1586+	DROP	R5	
000023A8	FEFDFCFB FAF9F8F7			1587	DC	XL16' FEFDFCFBFAF9F8F7 FFFFFFFFFFFFFFFFFF'	result
000023B0	FFFFFFFF FFFFFFFF						
000023B8	00000000 FEFDFCFB			1588	DC	XL16' 00000000FEFDFCFB 00000000FAF9F8F7'	v2
000023C0	00000000 FAF9F8F7						
000023C8	00001133 00005577			1589	DC	XL16' 0000113300005577 000099BB0000DDFF'	v3
000023D0	000099BB 0000DDFF						
000023D8				1590			
000023D8				1591	VRR_B	VPKLS, 3, 1	
000023D8		000023D8		1592+	DS	0FD	
000023D8	00002440			1593+	USING	*, R5	base for test data and test routine
000023DC	0019			1594+T25	DC	A(X25)	address of test routine
000023DE	00			1595+	DC	H' 25'	test number
000023DF	03			1596+	DC	X' 00'	
000023E0	01			1597+	DC	HL1' 3'	m4 used
000023E1	01			1598+	DC	HL1' 1'	m5 used
000023E2	0B			1599+	DC	HL1' 1'	CC
000023E4	00000000 00000000			1600+	DC	HL1' 11'	CC failed mask
000023EC	FF			1601+	DS	2F	extracted PSW after test (has CC)
000023ED	E5D7D2D3 E2404040			1602+	DC	X' FF'	extracted CC, if test failed
000023F8	00002470			1603+	DC	CL8' VPKLS'	instruction name
000023FC	00002480			1604+	DC	A(RE25)	address of v1 result
00002400	00002490			1605+	DC	A(RE25+16)	address of v2 source
00002404	00000010			1606+	DC	A(RE25+32)	address of v3 source
00002408	00002470			1607+	DC	A(16)	result length
00002410	00000000 00000000			1608+REA25	DC	A(RE25)	result address
00002418	00000000 00000000			1609+	DS	2FD	gap
00002420	00000000 00000000			1610+V1025	DS	XL16	V1 output
00002428	00000000 00000000						
00002430	00000000 00000000			1611+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002438	00000000 00000000			1612+*			
00002440				1613+X25	DS	0F	
00002440	E310 5024 0014		00000024	1614+	LGF	R1, V2ADDR	load v2 source
00002446	E761 0000 0806		00000000	1615+	VL	v22, 0(R1)	use v21 to test decoder
0000244C	E310 5028 0014		00000028	1616+	LGF	R1, V3ADDR	load v3 source
00002452	E771 0000 0806		00000000	1617+	VL	v23, 0(R1)	use v22 to test decoder
00002458	E756 7010 3E95			1618+	VPKLS	V21, V22, V23, 3, 1	test instruction
0000245E	B98D 0020			1619+	EPSW	R2, R0	extract psw
00002462	5020 500C		0000000C	1620+	ST	R2, CCPSW	to save CC
00002466	E750 5048 080E		00002420	1621+	VST	V21, V1025	save v1 output
0000246C	07FB			1622+	BR	R11	return
00002470				1623+RE25	DC	0F	V1 for this test
00002470				1624+	DROP	R5	
00002470	FFFFFFFF FFFFFFFF			1625	DC	XL16' FFFFFFFFFFFFFFFFFF FEFD FCFBFAF9F8F7'	result t
00002478	FEFD FCFB FAF9F8F7						
00002480	00001133 00005577			1626	DC	XL16' 0000113300005577 000099BB0000DDFF'	v2
00002488	000099BB 0000DDFF						
00002490	00000000 FEFD FCFB			1627	DC	XL16' 00000000FEFD FCFB 00000000FAF9F8F7'	v3
00002498	00000000 FAF9F8F7						
				1628			
000024A0				1629	VRR_B	VPKLS, 3, 3	
000024A0		000024A0		1630+	DS	0FD	
000024A0	00002508			1631+	USING	*, R5	base for test data and test routine
000024A4	001A			1632+T26	DC	A(X26)	address of test routine
000024A6	00			1633+	DC	H' 26'	test number
000024A7	03			1634+	DC	X' 00'	
000024A8	01			1635+	DC	HL1' 3'	m4 used
000024A9	03			1636+	DC	HL1' 1'	m5 used
000024AA	0E			1637+	DC	HL1' 3'	CC
000024AC	00000000 00000000			1638+	DC	HL1' 14'	CC failed mask
000024B4	FF			1639+	DS	2F	extracted PSW after test (has CC)
000024B5	E5D7D2D3 E2404040			1640+	DC	X' FF'	extracted CC, if test failed
000024C0	00002538			1641+	DC	CL8' VPKLS'	instruction name
000024C4	00002548			1642+	DC	A(RE26)	address of v1 result
000024C8	00002558			1643+	DC	A(RE26+16)	address of v2 source
000024CC	00000010			1644+	DC	A(RE26+32)	address of v3 source
000024D0	00002538			1645+	DC	A(16)	result length
000024D8	00000000 00000000			1646+REA26	DC	A(RE26)	result address
000024E0	00000000 00000000			1647+	DS	2FD	gap
000024E8	00000000 00000000			1648+V1026	DS	XL16	V1 output
000024F0	00000000 00000000						
000024F8	00000000 00000000			1649+	DS	2FD	gap
00002500	00000000 00000000						
				1650+*			
00002508				1651+X26	DS	0F	
00002508	E310 5024 0014		00000024	1652+	LGF	R1, V2ADDR	load v2 source
0000250E	E761 0000 0806		00000000	1653+	VL	v22, 0(R1)	use v21 to test decoder
00002514	E310 5028 0014		00000028	1654+	LGF	R1, V3ADDR	load v3 source
0000251A	E771 0000 0806		00000000	1655+	VL	v23, 0(R1)	use v22 to test decoder
00002520	E756 7010 3E95			1656+	VPKLS	V21, V22, V23, 3, 1	test instruction
00002526	B98D 0020			1657+	EPSW	R2, R0	extract psw
0000252A	5020 500C		0000000C	1658+	ST	R2, CCPSW	to save CC
0000252E	E750 5048 080E		000024E8	1659+	VST	V21, V1026	save v1 output
00002534	07FB			1660+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002538				1661+RE26	DC	0F	V1 for this test
00002538				1662+	DROP	R5	
00002538	FFFFFFFF FFFFFFFF			1663	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00002540	FFFFFFFF FFFFFFFF						
00002548	01110133 01550177			1664	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00002550	019901BB 01DD01FF						
00002558	01010203 04050607			1665	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00002560	08090A0B 0C0D0E0F						
				1666			
00002568				1667	VRR_B	VPKLS, 3, 3	
00002568		00002568		1668+	DS	0FD	
00002568	000025D0			1669+	USING	*, R5	base for test data and test routine
0000256C	001B			1670+T27	DC	A(X27)	address of test routine
0000256E	00			1671+	DC	H' 27'	test number
0000256F	03			1672+	DC	X' 00'	
00002570	01			1673+	DC	HL1' 3'	m4 used
00002571	03			1674+	DC	HL1' 1'	m5 used
00002572	0E			1675+	DC	HL1' 3'	CC
00002574	00000000 00000000			1676+	DC	HL1' 14'	CC failed mask
0000257C	FF			1677+	DS	2F	extracted PSW after test (has CC)
0000257D	E5D7D2D3 E2404040			1678+	DC	X' FF'	extracted CC, if test failed
00002588	00002600			1679+	DC	CL8' VPKLS'	instruction name
0000258C	00002610			1680+	DC	A(RE27)	address of v1 result
00002590	00002620			1681+	DC	A(RE27+16)	address of v2 source
00002594	00000010			1682+	DC	A(RE27+32)	address of v3 source
00002598	00002600			1683+	DC	A(16)	result length
000025A0	00000000 00000000			1684+REA27	DC	A(RE27)	result address
000025A8	00000000 00000000			1685+	DS	2FD	gap
000025B0	00000000 00000000			1686+V1027	DS	XL16	V1 output
000025B8	00000000 00000000						
000025C0	00000000 00000000			1687+	DS	2FD	gap
000025C8	00000000 00000000						
				1688+*			
000025D0				1689+X27	DS	0F	
000025D0	E310 5024 0014		00000024	1690+	LGF	R1, V2ADDR	load v2 source
000025D6	E761 0000 0806		00000000	1691+	VL	v22, 0(R1)	use v21 to test decoder
000025DC	E310 5028 0014		00000028	1692+	LGF	R1, V3ADDR	load v3 source
000025E2	E771 0000 0806		00000000	1693+	VL	v23, 0(R1)	use v22 to test decoder
000025E8	E756 7010 3E95			1694+	VPKLS	V21, V22, V23, 3, 1	test instruction
000025EE	B98D 0020			1695+	EPSW	R2, R0	extract psw
000025F2	5020 500C		0000000C	1696+	ST	R2, CCPSW	to save CC
000025F6	E750 5048 080E		000025B0	1697+	VST	V21, V1027	save v1 output
000025FC	07FB			1698+	BR	R11	return
00002600				1699+RE27	DC	0F	V1 for this test
00002600				1700+	DROP	R5	
00002600	FFFFFFFF FFFFFFFF			1701	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00002608	FFFFFFFF FFFFFFFF						
00002610	01010203 04050607			1702	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00002618	08090A0B 0C0D0E0F						
00002620	01110133 01550177			1703	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00002628	019901BB 01DD01FF						
				1704	*	-----	
				1705	*	mi sc. . .	
				1706	*	-----	
				1707	VRR_B	VPKLS, 1, 0	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002630				1708+	DS	0FD	
00002630		00002630		1709+	USING	*, R5	base for test data and test routine
00002630	00002698			1710+T28	DC	A(X28)	address of test routine
00002634	001C			1711+	DC	H' 28'	test number
00002636	00			1712+	DC	X' 00'	
00002637	01			1713+	DC	HL1' 1'	m4 used
00002638	01			1714+	DC	HL1' 1'	m5 used
00002639	00			1715+	DC	HL1' 0'	CC
0000263A	07			1716+	DC	HL1' 7'	CC failed mask
0000263C	00000000 00000000			1717+	DS	2F	extracted PSW after test (has CC)
00002644	FF			1718+	DC	X' FF'	extracted CC, if test failed
00002645	E5D7D2D3 E2404040			1719+	DC	CL8' VPKLS'	instruction name
00002650	000026C8			1720+	DC	A(RE28)	address of v1 result
00002654	000026D8			1721+	DC	A(RE28+16)	address of v2 source
00002658	000026E8			1722+	DC	A(RE28+32)	address of v3 source
0000265C	00000010			1723+	DC	A(16)	result length
00002660	000026C8			1724+REA28	DC	A(RE28)	result address
00002668	00000000 00000000			1725+	DS	2FD	gap
00002670	00000000 00000000						
00002678	00000000 00000000			1726+V1028	DS	XL16	V1 output
00002680	00000000 00000000						
00002688	00000000 00000000			1727+	DS	2FD	gap
00002690	00000000 00000000						
00002698				1728+*			
00002698	E310 5024 0014		00000024	1729+X28	DS	0F	
0000269E	E761 0000 0806		00000000	1730+	LGF	R1, V2ADDR	load v2 source
000026A4	E310 5028 0014		00000028	1731+	VL	v22, 0(R1)	use v21 to test decoder
000026AA	E771 0000 0806		00000000	1732+	LGF	R1, V3ADDR	load v3 source
000026B0	E756 7010 1E95			1733+	VL	v23, 0(R1)	use v22 to test decoder
000026B6	B98D 0020			1734+	VPKLS	V21, V22, V23, 1, 1	test instruction
000026B6	B98D 0020			1735+	EPSW	R2, R0	extract psw
000026BA	5020 500C		0000000C	1736+	ST	R2, CCPSW	to save CC
000026BE	E750 5048 080E		00002678	1737+	VST	V21, V1028	save v1 output
000026C4	07FB			1738+	BR	R11	return
000026C8				1739+RE28	DC	0F	V1 for this test
000026C8				1740+	DROP	R5	
000026C8	51535557 595B5D5F			1741	DC	XL16' 51535557 595B5D5F 61636567 696B6D6F'	result
000026D0	61636567 696B6D6F						
000026D8	00510053 00550057			1742	DC	XL16' 00510053 00550057 0059005B 005D005F'	v2
000026E0	0059005B 005D005F						
000026E8	00610063 00650067			1743	DC	XL16' 00610063 00650067 0069006B 006D006F'	v3
000026F0	0069006B 006D006F						
000026F8				1744			
000026F8				1745	VRR_B	VPKLS, 2, 0	
000026F8	00002760	000026F8		1746+	DS	0FD	
000026FC	001D			1747+	USING	*, R5	base for test data and test routine
000026FE	00			1748+T29	DC	A(X29)	address of test routine
000026FE	00			1749+	DC	H' 29'	test number
000026FF	02			1750+	DC	X' 00'	
00002700	01			1751+	DC	HL1' 2'	m4 used
00002701	00			1752+	DC	HL1' 1'	m5 used
00002701	00			1753+	DC	HL1' 0'	CC
00002702	07			1754+	DC	HL1' 7'	CC failed mask
00002704	00000000 00000000			1755+	DS	2F	extracted PSW after test (has CC)
0000270C	FF			1756+	DC	X' FF'	extracted CC, if test failed
0000270D	E5D7D2D3 E2404040			1757+	DC	CL8' VPKLS'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002718	00002790			1758+	DC	A(RE29)	address of v1 result
0000271C	000027A0			1759+	DC	A(RE29+16)	address of v2 source
00002720	000027B0			1760+	DC	A(RE29+32)	address of v3 source
00002724	00000010			1761+	DC	A(16)	result length
00002728	00002790			1762+REA29	DC	A(RE29)	result address
00002730	00000000 00000000			1763+	DS	2FD	gap
00002738	00000000 00000000						
00002740	00000000 00000000			1764+V1029	DS	XL16	V1 output
00002748	00000000 00000000						
00002750	00000000 00000000			1765+	DS	2FD	gap
00002758	00000000 00000000						
00002760				1766+*			
00002760	E310 5024 0014		00000024	1767+X29	DS	0F	
00002766	E761 0000 0806		00000000	1768+	LGF	R1, V2ADDR	load v2 source
0000276C	E310 5028 0014		00000028	1769+	VL	v22, 0(R1)	use v21 to test decoder
00002772	E771 0000 0806		00000000	1770+	LGF	R1, V3ADDR	load v3 source
00002778	E756 7010 2E95			1771+	VL	v23, 0(R1)	use v22 to test decoder
0000277E	B98D 0020			1772+	VPKLS	V21, V22, V23, 2, 1	test instruction
00002782	5020 500C		0000000C	1773+	EPSW	R2, R0	extract psw
00002786	E750 5048 080E		00002740	1774+	ST	R2, CCPSW	to save CC
0000278C	07FB			1775+	VST	V21, V1029	save v1 output
00002790				1776+	BR	R11	return
00002790				1777+RE29	DC	0F	V1 for this test
00002790				1778+	DROP	R5	
00002790	52535657 5A5B5E5F			1779	DC	XL16' 52535657 5A5B5E5F 62636667 6A6B6E6F'	result
00002798	62636667 6A6B6E6F						
000027A0	00005253 00005657			1780	DC	XL16' 00005253 00005657 00005A5B 00005E5F'	v2
000027A8	00005A5B 00005E5F						
000027B0	00006263 00006667			1781	DC	XL16' 00006263 00006667 00006A6B 00006E6F'	v3
000027B8	00006A6B 00006E6F						
000027C0				1782			
000027C0		000027C0		1783	VRR_B	VPKLS, 3, 0	
000027C0	00002828			1784+	DS	0FD	
000027C4	001E			1785+	USING	*, R5	base for test data and test routine
000027C6	00			1786+T30	DC	A(X30)	address of test routine
000027C7	03			1787+	DC	H' 30'	test number
000027C8	01			1788+	DC	X' 00'	
000027C9	00			1789+	DC	HL1' 3'	m4 used
000027CA	07			1790+	DC	HL1' 1'	m5 used
000027CC	00000000 00000000			1791+	DC	HL1' 0'	CC
000027D4	FF			1792+	DC	HL1' 7'	CC failed mask
000027D5	E5D7D2D3 E2404040			1793+	DS	2F	extracted PSW after test (has CC)
000027E0	00002858			1794+	DC	X' FF'	extracted CC, if test failed
000027E4	00002868			1795+	DC	CL8' VPKLS'	instruction name
000027E8	00002878			1796+	DC	A(RE30)	address of v1 result
000027EC	00000010			1797+	DC	A(RE30+16)	address of v2 source
000027F0	00002858			1798+	DC	A(RE30+32)	address of v3 source
000027F8	00000000 00000000			1799+	DC	A(16)	result length
00002800	00000000 00000000			1800+REA30	DC	A(RE30)	result address
00002808	00000000 00000000			1801+	DS	2FD	gap
00002810	00000000 00000000						
00002818	00000000 00000000			1802+V1030	DS	XL16	V1 output
00002820	00000000 00000000			1803+	DS	2FD	gap
				1804+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00002828				1805+X30	DS	0F			
00002828	E310 5024 0014		00000024	1806+	LGF	R1, V2ADDR	load v2 source		
0000282E	E761 0000 0806		00000000	1807+	VL	v22, 0(R1)	use v21 to test decoder		
00002834	E310 5028 0014		00000028	1808+	LGF	R1, V3ADDR	load v3 source		
0000283A	E771 0000 0806		00000000	1809+	VL	v23, 0(R1)	use v22 to test decoder		
00002840	E756 7010 3E95			1810+	VPKLS	V21, V22, V23, 3, 1	test instruction		
00002846	B98D 0020			1811+	EPSW	R2, R0	extract psw		
0000284A	5020 500C		0000000C	1812+	ST	R2, CCPSW	to save CC		
0000284E	E750 5048 080E		00002808	1813+	VST	V21, V1030	save v1 output		
00002854	07FB			1814+	BR	R11	return		
00002858				1815+RE30	DC	0F	V1 for this test		
00002858				1816+	DROP	R5			
00002858	54555657 5C5D5E5F			1817	DC	XL16' 54555657 5C5D5E5F 64656667 6C6D6E6F'	result		
00002860	64656667 6C6D6E6F								
00002868	00000000 54555657			1818	DC	XL16' 00000000 54555657 00000000 5C5D5E5F'	v2		
00002870	00000000 5C5D5E5F								
00002878	00000000 64656667			1819	DC	XL16' 00000000 64656667 00000000 6C6D6E6F'	v3		
00002880	00000000 6C6D6E6F								
				1820					
				1821 *					
				1822 *	VPKS	- Vector Pack Saturate			
				1823 *					
				1824 *	cc=0:	No saturation			
				1825 *	cc=1:	At least one but not all elements saturated			
				1826 *	cc=3:	Saturation on all elements			
				1827 *					
				1828 *	case -	simple cc debug			
				1829 *					
				1830 *	Halfword				
				1831	VRR_B	VPKS, 1, 0			
00002888				1832+	DS	0FD			
00002888		00002888		1833+	USING	*, R5	base for test data and test routine		
00002888	000028F0			1834+T31	DC	A(X31)	address of test routine		
0000288C	001F			1835+	DC	H' 31'	test number		
0000288E	00			1836+	DC	X' 00'			
0000288F	01			1837+	DC	HL1' 1'	m4 used		
00002890	01			1838+	DC	HL1' 1'	m5 used		
00002891	00			1839+	DC	HL1' 0'	CC		
00002892	07			1840+	DC	HL1' 7'	CC failed mask		
00002894	00000000 00000000			1841+	DS	2F	extracted PSW after test (has CC)		
0000289C	FF			1842+	DC	X' FF'	extracted CC, if test failed		
0000289D	E5D7D2E2 40404040			1843+	DC	CL8' VPKS'	instruction name		
000028A8	00002920			1844+	DC	A(RE31)	address of v1 result		
000028AC	00002930			1845+	DC	A(RE31+16)	address of v2 source		
000028B0	00002940			1846+	DC	A(RE31+32)	address of v3 source		
000028B4	00000010			1847+	DC	A(16)	result length		
000028B8	00002920			1848+REA31	DC	A(RE31)	result address		
000028C0	00000000 00000000			1849+	DS	2FD	gap		
000028C8	00000000 00000000								
000028D0	00000000 00000000			1850+V1031	DS	XL16	V1 output		
000028D8	00000000 00000000								
000028E0	00000000 00000000			1851+	DS	2FD	gap		
000028E8	00000000 00000000								
				1852+*					
000028F0				1853+X31	DS	0F			
000028F0	E310 5024 0014		00000024	1854+	LGF	R1, V2ADDR	load v2 source		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000028F6	E761 0000 0806		00000000	1855+	VL	v22, 0(R1)	use v21 to test decoder
000028FC	E310 5028 0014		00000028	1856+	LGF	R1, V3ADDR	load v3 source
00002902	E771 0000 0806		00000000	1857+	VL	v23, 0(R1)	use v22 to test decoder
00002908	E756 7010 1E97			1858+	VPKS	V21, V22, V23, 1, 1	test instruction
0000290E	B98D 0020			1859+	EPSW	R2, R0	extract psw
00002912	5020 500C		0000000C	1860+	ST	R2, CCPSW	to save CC
00002916	E750 5048 080E		000028D0	1861+	VST	V21, V1031	save v1 output
0000291C	07FB			1862+	BR	R11	return
00002920				1863+RE31	DC	0F	V1 for this test
00002920				1864+	DROP	R5	
00002920	00000000 00000000			1865	DC	XL16' 0000000000000000 0000000000000000'	result t
00002928	00000000 00000000						
00002930	00000000 00000000			1866	DC	XL16' 0000000000000000 0000000000000000'	v2
00002938	00000000 00000000						
00002940	00000000 00000000			1867	DC	XL16' 0000000000000000 0000000000000000'	v3
00002948	00000000 00000000						
				1868			
00002950				1869	VRR_B	VPKS, 1, 1	
00002950		00002950		1870+	DS	0FD	
00002950	000029B8			1871+	USING	*, R5	base for test data and test routine
00002954	0020			1872+T32	DC	A(X32)	address of test routine
00002956	00			1873+	DC	H' 32'	test number
00002956	00			1874+	DC	X' 00'	
00002957	01			1875+	DC	HL1' 1'	m4 used
00002958	01			1876+	DC	HL1' 1'	m5 used
00002959	01			1877+	DC	HL1' 1'	CC
0000295A	0B			1878+	DC	HL1' 11'	CC failed mask
0000295C	00000000 00000000			1879+	DS	2F	extracted PSW after test (has CC)
00002964	FF			1880+	DC	X' FF'	extracted CC, if test failed
00002965	E5D7D2E2 40404040			1881+	DC	CL8' VPKS'	instruction name
00002970	000029E8			1882+	DC	A(RE32)	address of v1 result
00002974	000029F8			1883+	DC	A(RE32+16)	address of v2 source
00002978	00002A08			1884+	DC	A(RE32+32)	address of v3 source
0000297C	00000010			1885+	DC	A(16)	result length
00002980	000029E8			1886+REA32	DC	A(RE32)	result address
00002988	00000000 00000000			1887+	DS	2FD	gap
00002990	00000000 00000000						
00002998	00000000 00000000			1888+V1032	DS	XL16	V1 output
000029A0	00000000 00000000						
000029A8	00000000 00000000			1889+	DS	2FD	gap
000029B0	00000000 00000000						
				1890+*			
000029B8				1891+X32	DS	0F	
000029B8	E310 5024 0014		00000024	1892+	LGF	R1, V2ADDR	load v2 source
000029BE	E761 0000 0806		00000000	1893+	VL	v22, 0(R1)	use v21 to test decoder
000029C4	E310 5028 0014		00000028	1894+	LGF	R1, V3ADDR	load v3 source
000029CA	E771 0000 0806		00000000	1895+	VL	v23, 0(R1)	use v22 to test decoder
000029D0	E756 7010 1E97			1896+	VPKS	V21, V22, V23, 1, 1	test instruction
000029D6	B98D 0020			1897+	EPSW	R2, R0	extract psw
000029DA	5020 500C		0000000C	1898+	ST	R2, CCPSW	to save CC
000029DE	E750 5048 080E		00002998	1899+	VST	V21, V1032	save v1 output
000029E4	07FB			1900+	BR	R11	return
000029E8				1901+RE32	DC	0F	V1 for this test
000029E8				1902+	DROP	R5	
000029E8	00000000 00000000			1903	DC	XL16' 0000000000000000 7F7F7F7F80808080'	result t
000029F0	7F7F7F7F 80808080						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000029F8	00000000 00000000			1904	DC	XL16' 0000000000000000 0000000000000000'	v2	
00002A00	00000000 00000000							
00002A08	0FFF0FFF 0FFF0FFF			1905	DC	XL16' 0FFF0FFF0FFF0FFF 8FFF8FFF8FFF8FFF'	v3	
00002A10	8FFF8FFF 8FFF8FFF							
				1906				
00002A18				1907	VRR_B	VPKS, 1, 3		
00002A18		00002A18		1908+	DS	0FD		
00002A18	00002A80			1909+	USING	*, R5	base for test data and test routine	
00002A1C	0021			1910+T33	DC	A(X33)	address of test routine	
00002A1E	00			1911+	DC	H' 33'	test number	
00002A1F	01			1912+	DC	X' 00'		
00002A20	01			1913+	DC	HL1' 1'	m4 used	
00002A21	03			1914+	DC	HL1' 1'	m5 used	
00002A22	0E			1915+	DC	HL1' 3'	CC	
00002A24	00000000 00000000			1916+	DC	HL1' 14'	CC failed mask	
00002A2C	FF			1917+	DS	2F	extracted PSW after test (has CC)	
00002A2D	E5D7D2E2 40404040			1918+	DC	X' FF'	extracted CC, if test failed	
00002A38	00002AB0			1919+	DC	CL8' VPKS'	instruction name	
00002A3C	00002AC0			1920+	DC	A(RE33)	address of v1 result	
00002A40	00002AD0			1921+	DC	A(RE33+16)	address of v2 source	
00002A44	00000010			1922+	DC	A(RE33+32)	address of v3 source	
00002A48	00002AB0			1923+	DC	A(16)	result length	
00002A50	00000000 00000000			1924+REA33	DC	A(RE33)	result address	
00002A58	00000000 00000000			1925+	DS	2FD	gap	
00002A60	00000000 00000000			1926+V1033	DS	XL16	V1 output	
00002A68	00000000 00000000							
00002A70	00000000 00000000			1927+	DS	2FD	gap	
00002A78	00000000 00000000							
				1928+*				
00002A80				1929+X33	DS	0F		
00002A80	E310 5024 0014		00000024	1930+	LGF	R1, V2ADDR	load v2 source	
00002A86	E761 0000 0806		00000000	1931+	VL	v22, 0(R1)	use v21 to test decoder	
00002A8C	E310 5028 0014		00000028	1932+	LGF	R1, V3ADDR	load v3 source	
00002A92	E771 0000 0806		00000000	1933+	VL	v23, 0(R1)	use v22 to test decoder	
00002A98	E756 7010 1E97			1934+	VPKS	V21, V22, V23, 1, 1	test instruction	
00002A9E	B98D 0020			1935+	EPSW	R2, R0	extract psw	
00002AA2	5020 500C		0000000C	1936+	ST	R2, CCPSW	to save CC	
00002AA6	E750 5048 080E		00002A60	1937+	VST	V21, V1033	save v1 output	
00002AAC	07FB			1938+	BR	R11	return	
00002AB0				1939+RE33	DC	0F	V1 for this test	
00002AB0				1940+	DROP	R5		
00002AB0	7F7F7F7F 80808080			1941	DC	XL16' 7F7F7F7F80808080 7F7F7F7F80808080'	result t	
00002AB8	7F7F7F7F 80808080							
00002AC0	0FFF0FFF 0FFF0FFF			1942	DC	XL16' 0FFF0FFF0FFF0FFF 8FFF8FFF8FFF8FFF'	v2	
00002AC8	8FFF8FFF 8FFF8FFF							
00002AD0	0FFF0FFF 0FFF0FFF			1943	DC	XL16' 0FFF0FFF0FFF0FFF 8FFF8FFF8FFF8FFF'	v3	
00002AD8	8FFF8FFF 8FFF8FFF							
				1944				
				1945 *Word				
00002AE0				1946	VRR_B	VPKS, 2, 0		
00002AE0		00002AE0		1947+	DS	0FD		
00002AE0	00002B48			1948+	USING	*, R5	base for test data and test routine	
00002AE4	0022			1949+T34	DC	A(X34)	address of test routine	
00002AE6	00			1950+	DC	H' 34'	test number	
				1951+	DC	X' 00'		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002AE7	02			1952+	DC	HL1' 2'	m4 used
00002AE8	01			1953+	DC	HL1' 1'	m5 used
00002AE9	00			1954+	DC	HL1' 0'	CC
00002AEA	07			1955+	DC	HL1' 7'	CC failed mask
00002AEC	00000000	00000000		1956+	DS	2F	extracted PSW after test (has CC)
00002AF4	FF			1957+	DC	X' FF'	extracted CC, if test failed
00002AF5	E5D7D2E2	40404040		1958+	DC	CL8' VPKS'	instruction name
00002B00	00002B78			1959+	DC	A(RE34)	address of v1 result
00002B04	00002B88			1960+	DC	A(RE34+16)	address of v2 source
00002B08	00002B98			1961+	DC	A(RE34+32)	address of v3 source
00002B0C	00000010			1962+	DC	A(16)	result length
00002B10	00002B78			1963+REA34	DC	A(RE34)	result address
00002B18	00000000	00000000		1964+	DS	2FD	gap
00002B20	00000000	00000000					
00002B28	00000000	00000000		1965+V1034	DS	XL16	V1 output
00002B30	00000000	00000000					
00002B38	00000000	00000000		1966+	DS	2FD	gap
00002B40	00000000	00000000					
00002B48				1967+*			
00002B48	E310 5024 0014		00000024	1968+X34	DS	0F	
00002B4E	E761 0000 0806		00000000	1969+	LGF	R1, V2ADDR	load v2 source
00002B54	E310 5028 0014		00000028	1970+	VL	v22, 0(R1)	use v21 to test decoder
00002B5A	E771 0000 0806		00000000	1971+	LGF	R1, V3ADDR	load v3 source
00002B60	E756 7010 2E97			1972+	VL	v23, 0(R1)	use v22 to test decoder
00002B66	B98D 0020			1973+	VPKS	V21, V22, V23, 2, 1	test instruction
00002B6A	5020 500C		0000000C	1974+	EPSW	R2, R0	extract psw
00002B6E	E750 5048 080E		00002B28	1975+	ST	R2, CCPSW	to save CC
00002B74	07FB			1976+	VST	V21, V1034	save v1 output
00002B78				1977+	BR	R11	return
00002B78				1978+RE34	DC	0F	V1 for this test
00002B78				1979+	DROP	R5	
00002B78	00000000	00000000		1980	DC	XL16' 0000000000000000 0000000000000000'	result
00002B80	00000000	00000000					
00002B88	00000000	00000000		1981	DC	XL16' 0000000000000000 0000000000000000'	v2
00002B90	00000000	00000000					
00002B98	00000000	00000000		1982	DC	XL16' 0000000000000000 0000000000000000'	v3
00002BA0	00000000	00000000					
00002BA8				1983			
00002BA8				1984	VRR_B	VPKS, 2, 1	
00002BA8		00002BA8		1985+	DS	0FD	
00002BA8	00002C10			1986+	USING	*, R5	base for test data and test routine
00002BAC	0023			1987+T35	DC	A(X35)	address of test routine
00002BAE	00			1988+	DC	H' 35'	test number
00002BAF	00			1989+	DC	X' 00'	
00002BAF	02			1990+	DC	HL1' 2'	m4 used
00002BB0	01			1991+	DC	HL1' 1'	m5 used
00002BB1	01			1992+	DC	HL1' 1'	CC
00002BB2	0B			1993+	DC	HL1' 11'	CC failed mask
00002BB4	00000000	00000000		1994+	DS	2F	extracted PSW after test (has CC)
00002BBC	FF			1995+	DC	X' FF'	extracted CC, if test failed
00002BBD	E5D7D2E2	40404040		1996+	DC	CL8' VPKS'	instruction name
00002BC8	00002C40			1997+	DC	A(RE35)	address of v1 result
00002BCC	00002C50			1998+	DC	A(RE35+16)	address of v2 source
00002BD0	00002C60			1999+	DC	A(RE35+32)	address of v3 source
00002BD4	00000010			2000+	DC	A(16)	result length
00002BD8	00002C40			2001+REA35	DC	A(RE35)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002BE0	00000000 00000000			2002+	DS	2FD	gap
00002BE8	00000000 00000000						
00002BF0	00000000 00000000			2003+V1035	DS	XL16	V1 output
00002BF8	00000000 00000000						
00002C00	00000000 00000000			2004+	DS	2FD	gap
00002C08	00000000 00000000						
00002C10				2005+*			
00002C10	E310 5024 0014		00000024	2006+X35	DS	0F	
00002C16	E761 0000 0806		00000000	2007+	LGF	R1, V2ADDR	load v2 source
00002C1C	E310 5028 0014		00000028	2008+	VL	v22, 0(R1)	use v21 to test decoder
00002C22	E771 0000 0806		00000000	2009+	LGF	R1, V3ADDR	load v3 source
00002C28	E756 7010 2E97			2010+	VL	v23, 0(R1)	use v22 to test decoder
00002C2E	B98D 0020			2011+	VPKS	V21, V22, V23, 2, 1	test instruction
00002C32	5020 500C		0000000C	2012+	EPSW	R2, R0	extract psw
00002C36	E750 5048 080E		00002BF0	2013+	ST	R2, CCPSW	to save CC
00002C3C	07FB			2014+	VST	V21, V1035	save v1 output
00002C40				2015+	BR	R11	return
00002C40				2016+RE35	DC	0F	V1 for this test
00002C40				2017+	DROP	R5	
00002C40	00000000 00000000			2018	DC	XL16' 0000000000000000 7FFF7FFF80008000'	result t
00002C48	7FFF7FFF 80008000						
00002C50	00000000 00000000			2019	DC	XL16' 0000000000000000 0000000000000000'	v2
00002C58	00000000 00000000						
00002C60	0000FFFF 0000FFFF			2020	DC	XL16' 0000FFFF0000FFFF 8FFF8FFF8FFF8FFF'	v3
00002C68	8FFF8FFF 8FFF8FFF						
00002C70				2021			
00002C70		00002C70		2022	VRR_B	VPKS, 2, 3	
00002C70	00002CD8			2023+	DS	0FD	
00002C74	0024			2024+	USING	*, R5	base for test data and test routine
00002C76	00			2025+T36	DC	A(X36)	address of test routine
00002C77	02			2026+	DC	H' 36'	test number
00002C78	01			2027+	DC	X' 00'	
00002C79	03			2028+	DC	HL1' 2'	m4 used
00002C7A	0E			2029+	DC	HL1' 1'	m5 used
00002C7C	00000000 00000000			2030+	DC	HL1' 3'	CC
00002C84	FF			2031+	DC	HL1' 14'	CC failed mask
00002C85	E5D7D2E2 40404040			2032+	DS	2F	extracted PSW after test (has CC)
00002C90	00002D08			2033+	DC	X' FF'	extracted CC, if test failed
00002C94	00002D18			2034+	DC	CL8' VPKS'	instruction name
00002C98	00002D28			2035+	DC	A(RE36)	address of v1 result
00002C9C	00000010			2036+	DC	A(RE36+16)	address of v2 source
00002CA0	00002D08			2037+	DC	A(RE36+32)	address of v3 source
00002CA8	00000000 00000000			2038+	DC	A(16)	result length
00002CB0	00000000 00000000			2039+REA36	DC	A(RE36)	result address
00002CB8	00000000 00000000			2040+	DS	2FD	gap
00002CC0	00000000 00000000			2041+V1036	DS	XL16	V1 output
00002CC8	00000000 00000000			2042+	DS	2FD	gap
00002CD0	00000000 00000000						
00002CD8				2043+*			
00002CD8	E310 5024 0014		00000024	2044+X36	DS	0F	
00002CDE	E761 0000 0806		00000000	2045+	LGF	R1, V2ADDR	load v2 source
00002CE4	E310 5028 0014		00000028	2046+	VL	v22, 0(R1)	use v21 to test decoder
00002CEA	E771 0000 0806		00000000	2047+	LGF	R1, V3ADDR	load v3 source
				2048+	VL	v23, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002CF0	E756 7010 2E97			2049+	VPKS	V21, V22, V23, 2, 1	test instruction	
00002CF6	B98D 0020			2050+	EPSW	R2, R0	extract psw	
00002CFA	5020 500C		0000000C	2051+	ST	R2, CCPSW	to save CC	
00002CFE	E750 5048 080E		00002CB8	2052+	VST	V21, V1036	save v1 output	
00002D04	07FB			2053+	BR	R11	return	
00002D08				2054+RE36	DC	0F	V1 for this test	
00002D08				2055+	DROP	R5		
00002D08	7FFF7FFF 80008000			2056	DC	XL16' 7FFF7FFF80008000 7FFF7FFF80008000'	result t	
00002D10	7FFF7FFF 80008000							
00002D18	0000FFFF 0000FFFF			2057	DC	XL16' 0000FFFF0000FFFF 8FFF8FFF8FFF8FFF'	v2	
00002D20	8FFF8FFF 8FFF8FFF							
00002D28	0000FFFF 0000FFFF			2058	DC	XL16' 0000FFFF0000FFFF 8FFF8FFF8FFF8FFF'	v3	
00002D30	8FFF8FFF 8FFF8FFF							
				2059				
				2060 *DoubleWord				
				2061	VRR_B	VPKS, 3, 0		
00002D38				2062+	DS	0FD		
00002D38		00002D38		2063+	USING	*, R5	base for test data and test routine	
00002D38	00002DA0			2064+T37	DC	A(X37)	address of test routine	
00002D3C	0025			2065+	DC	H' 37'	test number	
00002D3E	00			2066+	DC	X' 00'		
00002D3F	03			2067+	DC	HL1' 3'	m4 used	
00002D40	01			2068+	DC	HL1' 1'	m5 used	
00002D41	00			2069+	DC	HL1' 0'	CC	
00002D42	07			2070+	DC	HL1' 7'	CC failed mask	
00002D44	00000000 00000000			2071+	DS	2F	extracted PSW after test (has CC)	
00002D4C	FF			2072+	DC	X' FF'	extracted CC, if test failed	
00002D4D	E5D7D2E2 40404040			2073+	DC	CL8' VPKS'	instruction name	
00002D58	00002DD0			2074+	DC	A(RE37)	address of v1 result	
00002D5C	00002DE0			2075+	DC	A(RE37+16)	address of v2 source	
00002D60	00002DF0			2076+	DC	A(RE37+32)	address of v3 source	
00002D64	00000010			2077+	DC	A(16)	result length	
00002D68	00002DD0			2078+REA37	DC	A(RE37)	result address	
00002D70	00000000 00000000			2079+	DS	2FD	gap	
00002D78	00000000 00000000							
00002D80	00000000 00000000			2080+V1037	DS	XL16	V1 output	
00002D88	00000000 00000000							
00002D90	00000000 00000000			2081+	DS	2FD	gap	
00002D98	00000000 00000000							
				2082+*				
00002DA0				2083+X37	DS	0F		
00002DA0	E310 5024 0014		00000024	2084+	LGF	R1, V2ADDR	load v2 source	
00002DA6	E761 0000 0806		00000000	2085+	VL	v22, 0(R1)	use v21 to test decoder	
00002DAC	E310 5028 0014		00000028	2086+	LGF	R1, V3ADDR	load v3 source	
00002DB2	E771 0000 0806		00000000	2087+	VL	v23, 0(R1)	use v22 to test decoder	
00002DB8	E756 7010 3E97			2088+	VPKS	V21, V22, V23, 3, 1	test instruction	
00002DBE	B98D 0020			2089+	EPSW	R2, R0	extract psw	
00002DC2	5020 500C		0000000C	2090+	ST	R2, CCPSW	to save CC	
00002DC6	E750 5048 080E		00002D80	2091+	VST	V21, V1037	save v1 output	
00002DCC	07FB			2092+	BR	R11	return	
00002DD0				2093+RE37	DC	0F	V1 for this test	
00002DD0				2094+	DROP	R5		
00002DD0	00000000 00000000			2095	DC	XL16' 0000000000000000 0000000000000000'	result t	
00002DD8	00000000 00000000							
00002DE0	00000000 00000000			2096	DC	XL16' 0000000000000000 0000000000000000'	v2	
00002DE8	00000000 00000000							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002DF0	00000000 00000000			2097	DC	XL16' 0000000000000000 0000000000000000'	v3	
00002DF8	00000000 00000000							
				2098				
				2099	VRR_B	VPKS, 3, 1		
00002E00				2100+	DS	0FD		
00002E00		00002E00		2101+	USING	*, R5	base for test data and test routine	
00002E00	00002E68			2102+T38	DC	A(X38)	address of test routine	
00002E04	0026			2103+	DC	H' 38'	test number	
00002E06	00			2104+	DC	X' 00'		
00002E07	03			2105+	DC	HL1' 3'	m4 used	
00002E08	01			2106+	DC	HL1' 1'	m5 used	
00002E09	01			2107+	DC	HL1' 1'	CC	
00002E0A	0B			2108+	DC	HL1' 11'	CC failed mask	
00002E0C	00000000 00000000			2109+	DS	2F	extracted PSW after test (has CC)	
00002E14	FF			2110+	DC	X' FF'	extracted CC, if test failed	
00002E15	E5D7D2E2 40404040			2111+	DC	CL8' VPKS'	instruction name	
00002E20	00002E98			2112+	DC	A(RE38)	address of v1 result	
00002E24	00002EA8			2113+	DC	A(RE38+16)	address of v2 source	
00002E28	00002EB8			2114+	DC	A(RE38+32)	address of v3 source	
00002E2C	00000010			2115+	DC	A(16)	result length	
00002E30	00002E98			2116+REA38	DC	A(RE38)	result address	
00002E38	00000000 00000000			2117+	DS	2FD	gap	
00002E40	00000000 00000000							
00002E48	00000000 00000000			2118+V1038	DS	XL16	V1 output	
00002E50	00000000 00000000							
00002E58	00000000 00000000			2119+	DS	2FD	gap	
00002E60	00000000 00000000							
				2120+*				
00002E68				2121+X38	DS	0F		
00002E68	E310 5024 0014		00000024	2122+	LGF	R1, V2ADDR	load v2 source	
00002E6E	E761 0000 0806		00000000	2123+	VL	v22, 0(R1)	use v21 to test decoder	
00002E74	E310 5028 0014		00000028	2124+	LGF	R1, V3ADDR	load v3 source	
00002E7A	E771 0000 0806		00000000	2125+	VL	v23, 0(R1)	use v22 to test decoder	
00002E80	E756 7010 3E97			2126+	VPKS	V21, V22, V23, 3, 1	test instruction	
00002E86	B98D 0020			2127+	EPSW	R2, R0	extract psw	
00002E8A	5020 500C		0000000C	2128+	ST	R2, CCPSW	to save CC	
00002E8E	E750 5048 080E		00002E48	2129+	VST	V21, V1038	save v1 output	
00002E94	07FB			2130+	BR	R11	return	
00002E98				2131+RE38	DC	0F	V1 for this test	
00002E98				2132+	DROP	R5		
00002E98	00000000 7FFFFFFF			2133	DC	XL16' 000000007FFFFFFF 7FFFFFFF80000000'	result t	
00002EA0	7FFFFFFF 80000000							
00002EA8	00000000 00000000			2134	DC	XL16' 0000000000000000 0FFFFFFF80000000'	v2	
00002EB0	0FFFFFFF FFFFFFFF							
00002EB8	00000000 FFFFFFFF			2135	DC	XL16' 00000000FFFFFFF 8FFFFFFF80000000'	v3	
00002EC0	8FFFFFFF FFFFFFFF							
				2136				
				2137	VRR_B	VPKS, 3, 3		
00002EC8				2138+	DS	0FD		
00002EC8		00002EC8		2139+	USING	*, R5	base for test data and test routine	
00002EC8	00002F30			2140+T39	DC	A(X39)	address of test routine	
00002ECC	0027			2141+	DC	H' 39'	test number	
00002ECE	00			2142+	DC	X' 00'		
00002ECF	03			2143+	DC	HL1' 3'	m4 used	
00002ED0	01			2144+	DC	HL1' 1'	m5 used	
00002ED1	03			2145+	DC	HL1' 3'	CC	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002ED2	0E			2146+	DC	HL1' 14'	CC failed mask
00002ED4	00000000 00000000			2147+	DS	2F	extracted PSW after test (has CC)
00002EDC	FF			2148+	DC	X' FF'	extracted CC, if test failed
00002EDD	E5D7D2E2 40404040			2149+	DC	CL8' VPKS'	instruction name
00002EE8	00002F60			2150+	DC	A(RE39)	address of v1 result
00002EEC	00002F70			2151+	DC	A(RE39+16)	address of v2 source
00002EF0	00002F80			2152+	DC	A(RE39+32)	address of v3 source
00002EF4	00000010			2153+	DC	A(16)	result length
00002EF8	00002F60			2154+REA39	DC	A(RE39)	result address
00002F00	00000000 00000000			2155+	DS	2FD	gap
00002F08	00000000 00000000						
00002F10	00000000 00000000			2156+V1039	DS	XL16	V1 output
00002F18	00000000 00000000						
00002F20	00000000 00000000			2157+	DS	2FD	gap
00002F28	00000000 00000000						
00002F30				2158+*			
00002F30	E310 5024 0014		00000024	2159+X39	DS	0F	
00002F36	E761 0000 0806		00000000	2160+	LGF	R1, V2ADDR	load v2 source
00002F3C	E310 5028 0014		00000028	2161+	VL	v22, 0(R1)	use v21 to test decoder
00002F42	E771 0000 0806		00000000	2162+	LGF	R1, V3ADDR	load v3 source
00002F48	E756 7010 3E97			2163+	VL	v23, 0(R1)	use v22 to test decoder
00002F4E	B98D 0020			2164+	VPKS	V21, V22, V23, 3, 1	test instruction
00002F52	5020 500C		0000000C	2165+	EPSW	R2, R0	extract psw
00002F56	E750 5048 080E		00002F10	2166+	ST	R2, CCPSW	to save CC
00002F5C	07FB			2167+	VST	V21, V1039	save v1 output
00002F60				2168+	BR	R11	return
00002F60				2169+RE39	DC	0F	V1 for this test
00002F60				2170+	DROP	R5	
00002F60	7FFFFFFF 80000000			2171	DC	XL16' 7FFFFFFF80000000 7FFFFFFF80000000'	result t
00002F68	7FFFFFFF 80000000						
00002F70	000000FF FFFFFFFF			2172	DC	XL16' 000000FFFFFFFF 8FFFFFFFFFFFFFFFFF'	v2
00002F78	8FFFFFFFF FFFFFFFF						
00002F80	000000FF FFFFFFFF			2173	DC	XL16' 000000FFFFFFFF 8FFFFFFFFFFFFFFFFF'	v3
00002F88	8FFFFFFFF FFFFFFFF						
				2174			
				2175	*	-----	
				2176	*	case - general	
				2177	*	-----	
				2178	*	Hal fword	
				2179		VRR_B VPKS, 1, 0	
00002F90				2180+	DS	0FD	
00002F90		00002F90		2181+	USING	*, R5	base for test data and test routine
00002F90	00002FF8			2182+T40	DC	A(X40)	address of test routine
00002F94	0028			2183+	DC	H' 40'	test number
00002F96	00			2184+	DC	X' 00'	
00002F97	01			2185+	DC	HL1' 1'	m4 used
00002F98	01			2186+	DC	HL1' 1'	m5 used
00002F99	00			2187+	DC	HL1' 0'	CC
00002F9A	07			2188+	DC	HL1' 7'	CC failed mask
00002F9C	00000000 00000000			2189+	DS	2F	extracted PSW after test (has CC)
00002FA4	FF			2190+	DC	X' FF'	extracted CC, if test failed
00002FA5	E5D7D2E2 40404040			2191+	DC	CL8' VPKS'	instruction name
00002FB0	00003028			2192+	DC	A(RE40)	address of v1 result
00002FB4	00003038			2193+	DC	A(RE40+16)	address of v2 source
00002FB8	00003048			2194+	DC	A(RE40+32)	address of v3 source
00002FBC	00000010			2195+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002FC0	00003028			2196+REA40	DC	A(RE40)	result address
00002FC8	00000000 00000000			2197+	DS	2FD	gap
00002FD0	00000000 00000000						
00002FD8	00000000 00000000			2198+V1040	DS	XL16	V1 output
00002FE0	00000000 00000000						
00002FE8	00000000 00000000			2199+	DS	2FD	gap
00002FF0	00000000 00000000						
				2200+*			
00002FF8				2201+X40	DS	0F	
00002FF8	E310 5024 0014		00000024	2202+	LGF	R1, V2ADDR	load v2 source
00002FFE	E761 0000 0806		00000000	2203+	VL	v22, 0(R1)	use v21 to test decoder
00003004	E310 5028 0014		00000028	2204+	LGF	R1, V3ADDR	load v3 source
0000300A	E771 0000 0806		00000000	2205+	VL	v23, 0(R1)	use v22 to test decoder
00003010	E756 7010 1E97			2206+	VPKS	V21, V22, V23, 1, 1	test instruction
00003016	B98D 0020			2207+	EPSW	R2, R0	extract psw
0000301A	5020 500C		0000000C	2208+	ST	R2, CCPSW	to save CC
0000301E	E750 5048 080E		00002FD8	2209+	VST	V21, V1040	save v1 output
00003024	07FB			2210+	BR	R11	return
00003028				2211+RE40	DC	0F	V1 for this test
00003028				2212+	DROP	R5	
00003028	11335577 22446608			2213	DC	XL16' 1133557722446608 FEFDFCFBFAF9F8F7'	result
00003030	FEFDFCFB FAF9F8F7						
00003038	00110033 00550077			2214	DC	XL16' 0011003300550077 0022004400660008'	v2
00003040	00220044 00660008						
00003048	FFFEFFFD FFFCFFFB			2215	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00003050	FFFAFF9 FFF8FFF7						
				2216			
				2217	VRR_B	VPKS, 1, 0	
00003058				2218+	DS	0FD	
00003058		00003058		2219+	USING	*, R5	base for test data and test routine
00003058	000030C0			2220+T41	DC	A(X41)	address of test routine
0000305C	0029			2221+	DC	H' 41'	test number
0000305E	00			2222+	DC	X' 00'	
0000305F	01			2223+	DC	HL1' 1'	m4 used
00003060	01			2224+	DC	HL1' 1'	m5 used
00003061	00			2225+	DC	HL1' 0'	CC
00003062	07			2226+	DC	HL1' 7'	CC failed mask
00003064	00000000 00000000			2227+	DS	2F	extracted PSW after test (has CC)
0000306C	FF			2228+	DC	X' FF'	extracted CC, if test failed
0000306D	E5D7D2E2 40404040			2229+	DC	CL8' VPKS'	instruction name
00003078	000030F0			2230+	DC	A(RE41)	address of v1 result
0000307C	00003100			2231+	DC	A(RE41+16)	address of v2 source
00003080	00003110			2232+	DC	A(RE41+32)	address of v3 source
00003084	00000010			2233+	DC	A(16)	result length
00003088	000030F0			2234+REA41	DC	A(RE41)	result address
00003090	00000000 00000000			2235+	DS	2FD	gap
00003098	00000000 00000000						
000030A0	00000000 00000000			2236+V1041	DS	XL16	V1 output
000030A8	00000000 00000000						
000030B0	00000000 00000000			2237+	DS	2FD	gap
000030B8	00000000 00000000						
				2238+*			
000030C0				2239+X41	DS	0F	
000030C0	E310 5024 0014		00000024	2240+	LGF	R1, V2ADDR	load v2 source
000030C6	E761 0000 0806		00000000	2241+	VL	v22, 0(R1)	use v21 to test decoder
000030CC	E310 5028 0014		00000028	2242+	LGF	R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000030D2	E771 0000 0806		00000000	2243+	VL	v23, 0(R1)	use v22 to test decoder
000030D8	E756 7010 1E97			2244+	VPKS	V21, V22, V23, 1, 1	test instruction
000030DE	B98D 0020			2245+	EPSW	R2, R0	extract psw
000030E2	5020 500C		0000000C	2246+	ST	R2, CCPSW	to save CC
000030E6	E750 5048 080E		000030A0	2247+	VST	V21, V1041	save v1 output
000030EC	07FB			2248+	BR	R11	return
000030F0				2249+RE41	DC	0F	V1 for this test
000030F0				2250+	DROP	R5	
000030F0	FEFDFCFB FAF9F8F7			2251	DC	XL16' FEFDFCFBFAF9F8F7 1133557722446608'	result t
000030F8	11335577 22446608						
00003100	FFFEFFFD FFFCFFFB			2252	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00003108	FFFAFFF9 FFF8FFF7						
00003110	00110033 00550077			2253	DC	XL16' 0011003300550077 0022004400660008'	v3
00003118	00220044 00660008						
				2254			
				2255	VRR_B	VPKS, 1, 1	
00003120				2256+	DS	0FD	
00003120		00003120		2257+	USING	*, R5	base for test data and test routine
00003120	00003188			2258+T42	DC	A(X42)	address of test routine
00003124	002A			2259+	DC	H' 42'	test number
00003126	00			2260+	DC	X' 00'	
00003127	01			2261+	DC	HL1' 1'	m4 used
00003128	01			2262+	DC	HL1' 1'	m5 used
00003129	01			2263+	DC	HL1' 1'	CC
0000312A	0B			2264+	DC	HL1' 11'	CC failed mask
0000312C	00000000 00000000			2265+	DS	2F	extracted PSW after test (has CC)
00003134	FF			2266+	DC	X' FF'	extracted CC, if test failed
00003135	E5D7D2E2 40404040			2267+	DC	CL8' VPKS'	instruction name
00003140	000031B8			2268+	DC	A(RE42)	address of v1 result
00003144	000031C8			2269+	DC	A(RE42+16)	address of v2 source
00003148	000031D8			2270+	DC	A(RE42+32)	address of v3 source
0000314C	00000010			2271+	DC	A(16)	result length
00003150	000031B8			2272+REA42	DC	A(RE42)	result address
00003158	00000000 00000000			2273+	DS	2FD	gap
00003160	00000000 00000000						
00003168	00000000 00000000			2274+V1042	DS	XL16	V1 output
00003170	00000000 00000000						
00003178	00000000 00000000			2275+	DS	2FD	gap
00003180	00000000 00000000						
				2276+*			
00003188				2277+X42	DS	0F	
00003188	E310 5024 0014		00000024	2278+	LGF	R1, V2ADDR	load v2 source
0000318E	E761 0000 0806		00000000	2279+	VL	v22, 0(R1)	use v21 to test decoder
00003194	E310 5028 0014		00000028	2280+	LGF	R1, V3ADDR	load v3 source
0000319A	E771 0000 0806		00000000	2281+	VL	v23, 0(R1)	use v22 to test decoder
000031A0	E756 7010 1E97			2282+	VPKS	V21, V22, V23, 1, 1	test instruction
000031A6	B98D 0020			2283+	EPSW	R2, R0	extract psw
000031AA	5020 500C		0000000C	2284+	ST	R2, CCPSW	to save CC
000031AE	E750 5048 080E		00003168	2285+	VST	V21, V1042	save v1 output
000031B4	07FB			2286+	BR	R11	return
000031B8				2287+RE42	DC	0F	V1 for this test
000031B8				2288+	DROP	R5	
000031B8	017F7F7F 7F7F7F80			2289	DC	XL16' 017F7F7F7F7F7F80 1133557722446600'	result t
000031C0	11335577 22446600						
000031C8	00010203 04050607			2290	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2
000031D0	08090A0B 0C0DFE0F						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000031D8	00110033 00550077			2291	DC	XL16' 0011003300550077 0022004400660000'	v3	
000031E0	00220044 00660000							
				2292				
				2293	VRR_B	VPKS, 1, 1		
000031E8				2294+	DS	OFD		
000031E8		000031E8		2295+	USING	*, R5	base for test data and test routine	
000031E8	00003250			2296+T43	DC	A(X43)	address of test routine	
000031EC	002B			2297+	DC	H' 43'	test number	
000031EE	00			2298+	DC	X' 00'		
000031EF	01			2299+	DC	HL1' 1'	m4 used	
000031F0	01			2300+	DC	HL1' 1'	m5 used	
000031F1	01			2301+	DC	HL1' 1'	CC	
000031F2	0B			2302+	DC	HL1' 11'	CC failed mask	
000031F4	00000000 00000000			2303+	DS	2F	extracted PSW after test (has CC)	
000031FC	FF			2304+	DC	X' FF'	extracted CC, if test failed	
000031FD	E5D7D2E2 40404040			2305+	DC	CL8' VPKS'	instruction name	
00003208	00003280			2306+	DC	A(RE43)	address of v1 result	
0000320C	00003290			2307+	DC	A(RE43+16)	address of v2 source	
00003210	000032A0			2308+	DC	A(RE43+32)	address of v3 source	
00003214	00000010			2309+	DC	A(16)	result length	
00003218	00003280			2310+REA43	DC	A(RE43)	result address	
00003220	00000000 00000000			2311+	DS	2FD	gap	
00003228	00000000 00000000							
00003230	00000000 00000000		2312+V1043	DS	XL16	V1 output		
00003238	00000000 00000000							
00003240	00000000 00000000		2313+	DS	2FD	gap		
00003248	00000000 00000000							
				2314+*				
00003250				2315+X43	DS	0F		
00003250	E310 5024 0014		00000024	2316+	LGF	R1, V2ADDR	load v2 source	
00003256	E761 0000 0806		00000000	2317+	VL	v22, 0(R1)	use v21 to test decoder	
0000325C	E310 5028 0014		00000028	2318+	LGF	R1, V3ADDR	load v3 source	
00003262	E771 0000 0806		00000000	2319+	VL	v23, 0(R1)	use v22 to test decoder	
00003268	E756 7010 1E97			2320+	VPKS	V21, V22, V23, 1, 1	test instruction	
0000326E	B98D 0020			2321+	EPSW	R2, R0	extract psw	
00003272	5020 500C		0000000C	2322+	ST	R2, CCPSW	to save CC	
00003276	E750 5048 080E		00003230	2323+	VST	V21, V1043	save v1 output	
0000327C	07FB			2324+	BR	R11	return	
00003280				2325+RE43	DC	0F	V1 for this test	
00003280				2326+	DROP	R5		
00003280	11335577 22446600			2327	DC	XL16' 1133557722446600 017F7F7F7F7F80'	result t	
00003288	017F7F7F 7F7F7F80							
00003290	00110033 00550077			2328	DC	XL16' 0011003300550077 0022004400660000'	v2	
00003298	00220044 00660000							
000032A0	00010203 04050607			2329	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v3	
000032A8	08090A0B 0C0DFE0F							
				2330				
				2331	VRR_B	VPKS, 1, 3		
000032B0				2332+	DS	OFD		
000032B0		000032B0		2333+	USING	*, R5	base for test data and test routine	
000032B0	00003318			2334+T44	DC	A(X44)	address of test routine	
000032B4	002C			2335+	DC	H' 44'	test number	
000032B6	00			2336+	DC	X' 00'		
000032B7	01			2337+	DC	HL1' 1'	m4 used	
000032B8	01			2338+	DC	HL1' 1'	m5 used	
000032B9	03			2339+	DC	HL1' 3'	CC	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000032BA	0E			2340+	DC	HL1' 14'	CC failed mask
000032BC	00000000 00000000			2341+	DS	2F	extracted PSW after test (has CC)
000032C4	FF			2342+	DC	X' FF'	extracted CC, if test failed
000032C5	E5D7D2E2 40404040			2343+	DC	CL8' VPKS'	instruction name
000032D0	00003348			2344+	DC	A(RE44)	address of v1 result
000032D4	00003358			2345+	DC	A(RE44+16)	address of v2 source
000032D8	00003368			2346+	DC	A(RE44+32)	address of v3 source
000032DC	00000010			2347+	DC	A(16)	result length
000032E0	00003348			2348+REA44	DC	A(RE44)	result address
000032E8	00000000 00000000			2349+	DS	2FD	gap
000032F0	00000000 00000000						
000032F8	00000000 00000000			2350+V1044	DS	XL16	V1 output
00003300	00000000 00000000						
00003308	00000000 00000000			2351+	DS	2FD	gap
00003310	00000000 00000000						
				2352+*			
00003318				2353+X44	DS	0F	
00003318	E310 5024 0014		00000024	2354+	LGF	R1, V2ADDR	load v2 source
0000331E	E761 0000 0806		00000000	2355+	VL	v22, 0(R1)	use v21 to test decoder
00003324	E310 5028 0014		00000028	2356+	LGF	R1, V3ADDR	load v3 source
0000332A	E771 0000 0806		00000000	2357+	VL	v23, 0(R1)	use v22 to test decoder
00003330	E756 7010 1E97			2358+	VPKS	V21, V22, V23, 1, 1	test instruction
00003336	B98D 0020			2359+	EPSW	R2, R0	extract psw
0000333A	5020 500C		0000000C	2360+	ST	R2, CCPSW	to save CC
0000333E	E750 5048 080E		000032F8	2361+	VST	V21, V1044	save v1 output
00003344	07FB			2362+	BR	R11	return
00003348				2363+RE44	DC	0F	V1 for this test
00003348				2364+	DROP	R5	
00003348	7F7F7F7F 7F7F7F7F			2365	DC	XL16' 7F7F7F7F7F7F7F7F 7F7F7F7F7F7F7F7F'	result t
00003350	7F7F7F7F 7F7F7F7F						
00003358	01110133 01550177			2366	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00003360	019901BB 01DD01FF						
00003368	01010203 04050607			2367	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00003370	08090A0B 0C0D0E0F						
				2368			
00003378				2369	VRR_B	VPKS, 1, 3	
00003378		00003378		2370+	DS	0FD	
00003378	000033E0			2371+	USING	*, R5	base for test data and test routine
0000337C	002D			2372+T45	DC	A(X45)	address of test routine
0000337E	00			2373+	DC	H' 45'	test number
0000337F	01			2374+	DC	X' 00'	
00003380	01			2375+	DC	HL1' 1'	m4 used
00003381	03			2376+	DC	HL1' 1'	m5 used
00003382	0E			2377+	DC	HL1' 3'	CC
00003384	00000000 00000000			2378+	DC	HL1' 14'	CC failed mask
0000338C	FF			2379+	DS	2F	extracted PSW after test (has CC)
0000338D	E5D7D2E2 40404040			2380+	DC	X' FF'	extracted CC, if test failed
00003398	00003410			2381+	DC	CL8' VPKS'	instruction name
0000339C	00003420			2382+	DC	A(RE45)	address of v1 result
000033A0	00003430			2383+	DC	A(RE45+16)	address of v2 source
000033A4	00000010			2384+	DC	A(RE45+32)	address of v3 source
000033A8	00003410			2385+	DC	A(16)	result length
000033B0	00000000 00000000			2386+REA45	DC	A(RE45)	result address
000033B8	00000000 00000000			2387+	DS	2FD	gap
000033C0	00000000 00000000			2388+V1045	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000033C8	00000000 00000000						
000033D0	00000000 00000000			2389+	DS	2FD	gap
000033D8	00000000 00000000						
000033E0				2390+*			
000033E0	E310 5024 0014		00000024	2391+X45	DS	0F	
000033E6	E761 0000 0806		00000000	2392+	LGF	R1, V2ADDR	load v2 source
000033EC	E310 5028 0014		00000028	2393+	VL	v22, 0(R1)	use v21 to test decoder
000033F2	E771 0000 0806		00000000	2394+	LGF	R1, V3ADDR	load v3 source
000033F8	E756 7010 1E97			2395+	VL	v23, 0(R1)	use v22 to test decoder
000033FE	B98D 0020			2396+	VPKS	V21, V22, V23, 1, 1	test instruction
00003402	5020 500C		0000000C	2397+	EPSW	R2, R0	extract psw
00003406	E750 5048 080E		000033C0	2398+	ST	R2, CCPSW	to save CC
0000340C	07FB			2399+	VST	V21, V1045	save v1 output
00003410				2400+	BR	R11	return
00003410				2401+RE45	DC	0F	V1 for this test
00003410	7F7F7F7F 7F7F7F7F			2402+	DROP	R5	
00003410	7F7F7F7F 7F7F7F7F			2403	DC	XL16' 7F7F7F7F7F7F7F7F 7F7F7F7F7F7F7F7F'	result t
00003418	7F7F7F7F 7F7F7F7F						
00003420	01010203 04050607			2404	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00003428	08090A0B 0C0D0E0F						
00003430	01110133 01550177			2405	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00003438	019901BB 01DD01FF						
00003440				2406			
00003440				2407	VRR_B	VPKS, 1, 3	
00003440		00003440		2408+	DS	0FD	
00003440	000034A8			2409+	USING	*, R5	base for test data and test routine
00003444	002E			2410+T46	DC	A(X46)	address of test routine
00003446	00			2411+	DC	H' 46'	test number
00003446	00			2412+	DC	X' 00'	
00003447	01			2413+	DC	HL1' 1'	m4 used
00003448	01			2414+	DC	HL1' 1'	m5 used
00003449	03			2415+	DC	HL1' 3'	CC
0000344A	0E			2416+	DC	HL1' 14'	CC failed mask
0000344C	00000000 00000000			2417+	DS	2F	extracted PSW after test (has CC)
00003454	FF			2418+	DC	X' FF'	extracted CC, if test failed
00003455	E5D7D2E2 40404040			2419+	DC	CL8' VPKS'	instruction name
00003460	000034D8			2420+	DC	A(RE46)	address of v1 result
00003464	000034E8			2421+	DC	A(RE46+16)	address of v2 source
00003468	000034F8			2422+	DC	A(RE46+32)	address of v3 source
0000346C	00000010			2423+	DC	A(16)	result length
00003470	000034D8			2424+REA46	DC	A(RE46)	result address
00003478	00000000 00000000			2425+	DS	2FD	gap
00003480	00000000 00000000						
00003488	00000000 00000000			2426+V1046	DS	XL16	V1 output
00003490	00000000 00000000						
00003498	00000000 00000000			2427+	DS	2FD	gap
000034A0	00000000 00000000						
000034A8				2428+*			
000034A8	E310 5024 0014		00000024	2429+X46	DS	0F	
000034AE	E761 0000 0806		00000000	2430+	LGF	R1, V2ADDR	load v2 source
000034B4	E310 5028 0014		00000028	2431+	VL	v22, 0(R1)	use v21 to test decoder
000034BA	E771 0000 0806		00000000	2432+	LGF	R1, V3ADDR	load v3 source
000034C0	E756 7010 1E97			2433+	VL	v23, 0(R1)	use v22 to test decoder
000034C6	B98D 0020			2434+	VPKS	V21, V22, V23, 1, 1	test instruction
000034CA	5020 500C		0000000C	2435+	EPSW	R2, R0	extract psw
				2436+	ST	R2, CCPSW	to save CC

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000034CE	E750 5048 080E		00003488	2437+	VST	V21, V1046	save v1 output	
000034D4	07FB			2438+	BR	R11	return	
000034D8				2439+RE46	DC	0F	V1 for this test	
000034D8				2440+	DROP	R5		
000034D8	80808080 80808080			2441	DC	XL16' 8080808080808080 8080808080808080'	result	t
000034E0	80808080 80808080							
000034E8	F111F133 F155F177			2442	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v2	
000034F0	F199F1BB F1DDF1FF							
000034F8	F101F203 F405F607			2443	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v3	
00003500	F809FAFB FCFDFE0F							
				2444				
00003508				2445	VRR_B	VPKS, 1, 3		
00003508		00003508		2446+	DS	0FD		
00003508	00003570			2447+	USING	*, R5	base for test data and test routine	
0000350C	002F			2448+T47	DC	A(X47)	address of test routine	
0000350E	00			2449+	DC	H' 47'	test number	
0000350F	01			2450+	DC	X' 00'		
00003510	01			2451+	DC	HL1' 1'	m4 used	
00003511	03			2452+	DC	HL1' 1'	m5 used	
00003512	0E			2453+	DC	HL1' 3'	CC	
00003514	00000000 00000000			2454+	DC	HL1' 14'	CC failed mask	
0000351C	FF			2455+	DS	2F	extracted PSW after test (has CC)	
0000351D	E5D7D2E2 40404040			2456+	DC	X' FF'	extracted CC, if test failed	
00003528	000035A0			2457+	DC	CL8' VPKS'	instruction name	
0000352C	000035B0			2458+	DC	A(RE47)	address of v1 result	
00003530	000035C0			2459+	DC	A(RE47+16)	address of v2 source	
00003534	00000010			2460+	DC	A(RE47+32)	address of v3 source	
00003538	000035A0			2461+	DC	A(16)	result length	
00003540	00000000 00000000			2462+REA47	DC	A(RE47)	result address	
00003548	00000000 00000000			2463+	DS	2FD	gap	
00003550	00000000 00000000			2464+V1047	DS	XL16	V1 output	
00003558	00000000 00000000							
00003560	00000000 00000000			2465+	DS	2FD	gap	
00003568	00000000 00000000							
				2466+*				
00003570				2467+X47	DS	0F		
00003570	E310 5024 0014	00000024		2468+	LGF	R1, V2ADDR	load v2 source	
00003576	E761 0000 0806	00000000		2469+	VL	v22, 0(R1)	use v21 to test decoder	
0000357C	E310 5028 0014	00000028		2470+	LGF	R1, V3ADDR	load v3 source	
00003582	E771 0000 0806	00000000		2471+	VL	v23, 0(R1)	use v22 to test decoder	
00003588	E756 7010 1E97			2472+	VPKS	V21, V22, V23, 1, 1	test instruction	
0000358E	B98D 0020			2473+	EPSW	R2, R0	extract psw	
00003592	5020 500C	0000000C		2474+	ST	R2, CCPSW	to save CC	
00003596	E750 5048 080E	00003550		2475+	VST	V21, V1047	save v1 output	
0000359C	07FB			2476+	BR	R11	return	
000035A0				2477+RE47	DC	0F	V1 for this test	
000035A0				2478+	DROP	R5		
000035A0	80808080 80808080			2479	DC	XL16' 8080808080808080 8080808080808080'	result	t
000035A8	80808080 80808080							
000035B0	F101F203 F405F607			2480	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v2	
000035B8	F809FAFB FCFDFE0F							
000035C0	F111F133 F155F177			2481	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v3	
000035C8	F199F1BB F1DDF1FF							
				2482				
				2483	*Word			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000035D0				2484	VRR_B	VPKS, 2, 0	
000035D0				2485+	DS	0FD	
000035D0		000035D0		2486+	USING	*, R5	base for test data and test routine
000035D0	00003638			2487+T48	DC	A(X48)	address of test routine
000035D4	0030			2488+	DC	H' 48'	test number
000035D6	00			2489+	DC	X' 00'	
000035D7	02			2490+	DC	HL1' 2'	m4 used
000035D8	01			2491+	DC	HL1' 1'	m5 used
000035D9	00			2492+	DC	HL1' 0'	CC
000035DA	07			2493+	DC	HL1' 7'	CC failed mask
000035DC	00000000 00000000			2494+	DS	2F	extracted PSW after test (has CC)
000035E4	FF			2495+	DC	X' FF'	extracted CC, if test failed
000035E5	E5D7D2E2 40404040			2496+	DC	CL8' VPKS'	instruction name
000035F0	00003668			2497+	DC	A(RE48)	address of v1 result
000035F4	00003678			2498+	DC	A(RE48+16)	address of v2 source
000035F8	00003688			2499+	DC	A(RE48+32)	address of v3 source
000035FC	00000010			2500+	DC	A(16)	result length
00003600	00003668			2501+REA48	DC	A(RE48)	result address
00003608	00000000 00000000			2502+	DS	2FD	gap
00003610	00000000 00000000						
00003618	00000000 00000000			2503+V1048	DS	XL16	V1 output
00003620	00000000 00000000						
00003628	00000000 00000000			2504+	DS	2FD	gap
00003630	00000000 00000000						
				2505+*			
00003638				2506+X48	DS	0F	
00003638	E310 5024 0014		00000024	2507+	LGF	R1, V2ADDR	load v2 source
0000363E	E761 0000 0806		00000000	2508+	VL	v22, 0(R1)	use v21 to test decoder
00003644	E310 5028 0014		00000028	2509+	LGF	R1, V3ADDR	load v3 source
0000364A	E771 0000 0806		00000000	2510+	VL	v23, 0(R1)	use v22 to test decoder
00003650	E756 7010 2E97			2511+	VPKS	V21, V22, V23, 2, 1	test instruction
00003656	B98D 0020			2512+	EPSW	R2, R0	extract psw
0000365A	5020 500C		0000000C	2513+	ST	R2, CCPSW	to save CC
0000365E	E750 5048 080E		00003618	2514+	VST	V21, V1048	save v1 output
00003664	07FB			2515+	BR	R11	return
00003668				2516+RE48	DC	0F	V1 for this test
00003668				2517+	DROP	R5	
00003668	11335577 22446688			2518	DC	XL16' 1133557722446688 FEFDFCFBFAF9F8F7'	result
00003670	FEFDFCFB FAF9F8F7						
00003678	00001133 00005577			2519	DC	XL16' 0000113300005577 0000224400006688'	v2
00003680	00002244 00006688						
00003688	FFFFFFFD FFFFCFB			2520	DC	XL16' FFFFFFFDFFFFFFCFB FFFFAF9FFFFFFF8F7'	v3
00003690	FFFFFAF9 FFFFF8F7						
				2521			
00003698				2522	VRR_B	VPKS, 2, 0	
00003698		00003698		2523+	DS	0FD	
00003698	00003700			2524+	USING	*, R5	base for test data and test routine
0000369C	0031			2525+T49	DC	A(X49)	address of test routine
0000369E	00			2526+	DC	H' 49'	test number
0000369F	00			2527+	DC	X' 00'	
000036A0	02			2528+	DC	HL1' 2'	m4 used
000036A0	01			2529+	DC	HL1' 1'	m5 used
000036A1	00			2530+	DC	HL1' 0'	CC
000036A2	07			2531+	DC	HL1' 7'	CC failed mask
000036A4	00000000 00000000			2532+	DS	2F	extracted PSW after test (has CC)
000036AC	FF			2533+	DC	X' FF'	extracted CC, if test failed

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000036AD	E5D7D2E2 40404040			2534+	DC	CL8' VPKS'	instruction name
000036B8	00003730			2535+	DC	A(RE49)	address of v1 result
000036BC	00003740			2536+	DC	A(RE49+16)	address of v2 source
000036C0	00003750			2537+	DC	A(RE49+32)	address of v3 source
000036C4	00000010			2538+	DC	A(16)	result length
000036C8	00003730			2539+REA49	DC	A(RE49)	result address
000036D0	00000000 00000000			2540+	DS	2FD	gap
000036D8	00000000 00000000						
000036E0	00000000 00000000			2541+V1049	DS	XL16	V1 output
000036E8	00000000 00000000						
000036F0	00000000 00000000			2542+	DS	2FD	gap
000036F8	00000000 00000000						
00003700				2543+*			
00003700	E310 5024 0014		00000024	2544+X49	DS	0F	
00003706	E761 0000 0806		00000000	2545+	LGF	R1, V2ADDR	load v2 source
0000370C	E310 5028 0014		00000028	2546+	VL	v22, 0(R1)	use v21 to test decoder
00003712	E771 0000 0806		00000000	2547+	LGF	R1, V3ADDR	load v3 source
00003718	E756 7010 2E97			2548+	VL	v23, 0(R1)	use v22 to test decoder
0000371E	B98D 0020			2549+	VPKS	V21, V22, V23, 2, 1	test instruction
00003722	5020 500C		0000000C	2550+	EPSW	R2, R0	extract psw
00003726	E750 5048 080E		000036E0	2551+	ST	R2, CCPSW	to save CC
0000372C	07FB			2552+	VST	V21, V1049	save v1 output
00003730				2553+	BR	R11	return
00003730				2554+REA49	DC	0F	V1 for this test
00003730				2555+	DROP	R5	
00003730	FEFDFCFB FAF9F8F7			2556	DC	XL16' FEFDFCFBFAF9F8F7 1133557722446688'	result t
00003738	11335577 22446688						
00003740	FFFFFFFD FFFFCFB			2557	DC	XL16' FFFFFFFEFDFFFFFFCFB FFFFFAF9FFFFFFF8F7'	v2
00003748	FFFFFFAF9 FFFFF8F7						
00003750	00001133 00005577			2558	DC	XL16' 0000113300005577 0000224400006688'	v3
00003758	00002244 00006688						
00003760				2559			
00003760		00003760		2560	VRR_B	VPKS, 2, 1	
00003760	000037C8			2561+	DS	0FD	
00003764	0032			2562+	USING	*, R5	base for test data and test routine
00003766	00			2563+T50	DC	A(X50)	address of test routine
00003767	02			2564+	DC	H' 50'	test number
00003768	01			2565+	DC	X' 00'	
00003769	01			2566+	DC	HL1' 2'	m4 used
0000376A	0B			2567+	DC	HL1' 1'	m5 used
0000376C	00000000 00000000			2568+	DC	HL1' 1'	CC
00003774	FF			2569+	DC	HL1' 11'	CC failed mask
00003775	E5D7D2E2 40404040			2570+	DS	2F	extracted PSW after test (has CC)
00003780	000037F8			2571+	DC	X' FF'	extracted CC, if test failed
00003784	00003808			2572+	DC	CL8' VPKS'	instruction name
00003788	00003818			2573+	DC	A(RE50)	address of v1 result
0000378C	00000010			2574+	DC	A(RE50+16)	address of v2 source
00003790	000037F8			2575+	DC	A(RE50+32)	address of v3 source
00003798	00000000 00000000			2576+	DC	A(16)	result length
000037A0	00000000 00000000			2577+REA50	DC	A(RE50)	result address
000037A8	00000000 00000000			2578+	DS	2FD	gap
000037B0	00000000 00000000						
000037B8	00000000 00000000			2579+V1050	DS	XL16	V1 output
000037C0	00000000 00000000			2580+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000037C8				2581+*			
000037C8	E310 5024 0014		00000024	2582+X50	DS	0F	
000037CE	E761 0000 0806		00000000	2583+	LGF	R1, V2ADDR	load v2 source
000037D4	E310 5028 0014		00000028	2584+	VL	v22, 0(R1)	use v21 to test decoder
000037DA	E771 0000 0806		00000000	2585+	LGF	R1, V3ADDR	load v3 source
000037E0	E756 7010 2E97			2586+	VL	v23, 0(R1)	use v22 to test decoder
000037E6	B98D 0020			2587+	VPKS	V21, V22, V23, 2, 1	test instruction
000037EA	5020 500C		0000000C	2588+	EPSW	R2, R0	extract psw
000037EE	E750 5048 080E		000037A8	2589+	ST	R2, CCPSW	to save CC
000037F4	07FB			2590+	VST	V21, V1050	save v1 output
000037F8				2591+	BR	R11	return
000037F8				2592+RE50	DC	0F	V1 for this test
000037F8	12037FFF 7FFF7FFF			2593+	DROP	R5	
00003800	11335577 19BB2DFF			2594	DC	XL16' 12037FFF7FFF7FFF 1133557719BB2DFF'	result t
00003808	00001203 04050607			2595	DC	XL16' 0000120304050607 08090A0B0C0D0E0F'	v2
00003810	08090A0B 0C0D0E0F						
00003818	00001133 00005577			2596	DC	XL16' 0000113300005577 000019BB00002DFF'	v3
00003820	000019BB 00002DFF						
00003828				2597			
00003828		00003828		2598	VRR_B	VPKS, 2, 1	
00003828	00003890			2599+	DS	0FD	
0000382C	0033			2600+	USING	*, R5	base for test data and test routine
0000382E	00			2601+T51	DC	A(X51)	address of test routine
0000382F	02			2602+	DC	H' 51'	test number
00003830	01			2603+	DC	X' 00'	
00003831	01			2604+	DC	HL1' 2'	m4 used
00003832	0B			2605+	DC	HL1' 1'	m5 used
00003833	0B			2606+	DC	HL1' 1'	CC
00003834	00000000 00000000			2607+	DC	HL1' 11'	CC failed mask
0000383C	FF			2608+	DS	2F	extracted PSW after test (has CC)
0000383D	E5D7D2E2 40404040			2609+	DC	X' FF'	extracted CC, if test failed
00003848	000038C0			2610+	DC	CL8' VPKS'	instruction name
0000384C	000038D0			2611+	DC	A(RE51)	address of v1 result
00003850	000038E0			2612+	DC	A(RE51+16)	address of v2 source
00003854	00000010			2613+	DC	A(RE51+32)	address of v3 source
00003858	000038C0			2614+	DC	A(16)	result length
00003860	00000000 00000000			2615+REA51	DC	A(RE51)	result address
00003868	00000000 00000000			2616+	DS	2FD	gap
00003870	00000000 00000000			2617+V1051	DS	XL16	V1 output
00003878	00000000 00000000						
00003880	00000000 00000000			2618+	DS	2FD	gap
00003888	00000000 00000000						
00003890				2619+*			
00003890	E310 5024 0014		00000024	2620+X51	DS	0F	
00003896	E761 0000 0806		00000000	2621+	LGF	R1, V2ADDR	load v2 source
0000389C	E310 5028 0014		00000028	2622+	VL	v22, 0(R1)	use v21 to test decoder
000038A2	E771 0000 0806		00000000	2623+	LGF	R1, V3ADDR	load v3 source
000038A8	E756 7010 2E97			2624+	VL	v23, 0(R1)	use v22 to test decoder
000038AE	B98D 0020			2625+	VPKS	V21, V22, V23, 2, 1	test instruction
000038B2	5020 500C		0000000C	2626+	EPSW	R2, R0	extract psw
000038B6	E750 5048 080E		00003870	2627+	ST	R2, CCPSW	to save CC
000038BC	07FB			2628+	VST	V21, V1051	save v1 output
000038C0				2629+	BR	R11	return
				2630+RE51	DC	0F	V1 for this test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000038C0				2631+	DROP	R5		
000038C0	11335577 19BB2DFF			2632	DC	XL16' 1133557719BB2DFF 12037FFF7FFF7FFF'	result	t
000038C8	12037FFF 7FFF7FFF							
000038D0	00001133 00005577			2633	DC	XL16' 0000113300005577 000019BB00002DFF'	v2	
000038D8	000019BB 00002DFF							
000038E0	00001203 04050607			2634	DC	XL16' 0000120304050607 08090A0B0C0D0E0F'	v3	
000038E8	08090A0B 0C0D0E0F							
				2635				
000038F0				2636	VRR_B	VPKS, 2, 3		
000038F0		000038F0		2637+	DS	0FD		
000038F0	00003958			2638+	USING	*, R5	base for test data and test routine	
000038F4	0034			2639+T52	DC	A(X52)	address of test routine	
000038F6	00			2640+	DC	H' 52'	test number	
000038F7	02			2641+	DC	X' 00'		
000038F8	01			2642+	DC	HL1' 2'	m4 used	
000038F9	03			2643+	DC	HL1' 1'	m5 used	
000038FA	0E			2644+	DC	HL1' 3'	CC	
000038FA	0E			2645+	DC	HL1' 14'	CC failed mask	
000038FC	00000000 00000000			2646+	DS	2F	extracted PSW after test (has CC)	
00003904	FF			2647+	DC	X' FF'	extracted CC, if test failed	
00003905	E5D7D2E2 40404040			2648+	DC	CL8' VPKS'	instruction name	
00003910	00003988			2649+	DC	A(RE52)	address of v1 result	
00003914	00003998			2650+	DC	A(RE52+16)	address of v2 source	
00003918	000039A8			2651+	DC	A(RE52+32)	address of v3 source	
0000391C	00000010			2652+	DC	A(16)	result length	
00003920	00003988			2653+REA52	DC	A(RE52)	result address	
00003928	00000000 00000000			2654+	DS	2FD	gap	
00003930	00000000 00000000							
00003938	00000000 00000000			2655+V1052	DS	XL16	V1 output	
00003940	00000000 00000000							
00003948	00000000 00000000			2656+	DS	2FD	gap	
00003950	00000000 00000000							
				2657+*				
00003958				2658+X52	DS	0F		
00003958	E310 5024 0014		00000024	2659+	LGF	R1, V2ADDR	load v2 source	
0000395E	E761 0000 0806		00000000	2660+	VL	v22, 0(R1)	use v21 to test decoder	
00003964	E310 5028 0014		00000028	2661+	LGF	R1, V3ADDR	load v3 source	
0000396A	E771 0000 0806		00000000	2662+	VL	v23, 0(R1)	use v22 to test decoder	
00003970	E756 7010 2E97			2663+	VPKS	V21, V22, V23, 2, 1	test instruction	
00003976	B98D 0020			2664+	EPSW	R2, R0	extract psw	
0000397A	5020 500C		0000000C	2665+	ST	R2, CCPSW	to save CC	
0000397E	E750 5048 080E		00003938	2666+	VST	V21, V1052	save v1 output	
00003984	07FB			2667+	BR	R11	return	
00003988				2668+RE52	DC	0F	V1 for this test	
00003988				2669+	DROP	R5		
00003988	7FFF7FFF 7FFF7FFF			2670	DC	XL16' 7FFF7FFF7FFF7FFF 7FFF7FFF7FFF7FFF'	result	t
00003990	7FFF7FFF 7FFF7FFF							
00003998	01110133 01550177			2671	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2	
000039A0	019901BB 01DD01FF							
000039A8	01010203 04050607			2672	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3	
000039B0	08090A0B 0C0D0E0F							
				2673				
000039B8				2674	VRR_B	VPKS, 2, 3		
000039B8		000039B8		2675+	DS	0FD		
000039B8	00003A20			2676+	USING	*, R5	base for test data and test routine	
				2677+T53	DC	A(X53)	address of test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000039BC	0035			2678+	DC	H' 53'	test number
000039BE	00			2679+	DC	X' 00'	
000039BF	02			2680+	DC	HL1' 2'	m4 used
000039C0	01			2681+	DC	HL1' 1'	m5 used
000039C1	03			2682+	DC	HL1' 3'	CC
000039C2	0E			2683+	DC	HL1' 14'	CC failed mask
000039C4	00000000 00000000			2684+	DS	2F	extracted PSW after test (has CC)
000039CC	FF			2685+	DC	X' FF'	extracted CC, if test failed
000039CD	E5D7D2E2 40404040			2686+	DC	CL8' VPKS'	instruction name
000039D8	00003A50			2687+	DC	A(RE53)	address of v1 result
000039DC	00003A60			2688+	DC	A(RE53+16)	address of v2 source
000039E0	00003A70			2689+	DC	A(RE53+32)	address of v3 source
000039E4	00000010			2690+	DC	A(16)	result length
000039E8	00003A50			2691+REA53	DC	A(RE53)	result address
000039F0	00000000 00000000			2692+	DS	2FD	gap
000039F8	00000000 00000000						
00003A00	00000000 00000000			2693+V1053	DS	XL16	V1 output
00003A08	00000000 00000000						
00003A10	00000000 00000000			2694+	DS	2FD	gap
00003A18	00000000 00000000						
00003A20				2695+*			
00003A20	E310 5024 0014		00000024	2696+X53	DS	0F	
00003A26	E761 0000 0806		00000000	2697+	LGF	R1, V2ADDR	load v2 source
00003A2C	E310 5028 0014		00000028	2698+	VL	v22, 0(R1)	use v21 to test decoder
00003A32	E771 0000 0806		00000000	2699+	LGF	R1, V3ADDR	load v3 source
00003A38	E756 7010 2E97		00000000	2700+	VL	v23, 0(R1)	use v22 to test decoder
00003A3E	B98D 0020			2701+	VPKS	V21, V22, V23, 2, 1	test instruction
00003A3E	B98D 0020			2702+	EPSW	R2, R0	extract psw
00003A42	5020 500C		0000000C	2703+	ST	R2, CCPSW	to save CC
00003A46	E750 5048 080E		00003A00	2704+	VST	V21, V1053	save v1 output
00003A4C	07FB			2705+	BR	R11	return
00003A50				2706+RE53	DC	0F	V1 for this test
00003A50				2707+	DROP	R5	
00003A50	7FFF7FFF 7FFF7FFF			2708	DC	XL16' 7FFF7FFF7FFF7FFF 7FFF7FFF7FFF7FFF'	result t
00003A58	7FFF7FFF 7FFF7FFF						
00003A60	01010203 04050607			2709	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
00003A68	08090A0B 0C0D0E0F						
00003A70	01110133 01550177			2710	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00003A78	019901BB 01DD01FF						
00003A80				2711			
00003A80				2712	VRR_B	VPKS, 2, 3	
00003A80		00003A80		2713+	DS	0FD	
00003A80	00003AE8			2714+	USING	*, R5	base for test data and test routine
00003A84	0036			2715+T54	DC	A(X54)	address of test routine
00003A86	00			2716+	DC	H' 54'	test number
00003A86	00			2717+	DC	X' 00'	
00003A87	02			2718+	DC	HL1' 2'	m4 used
00003A88	01			2719+	DC	HL1' 1'	m5 used
00003A89	03			2720+	DC	HL1' 3'	CC
00003A8A	0E			2721+	DC	HL1' 14'	CC failed mask
00003A8C	00000000 00000000			2722+	DS	2F	extracted PSW after test (has CC)
00003A94	FF			2723+	DC	X' FF'	extracted CC, if test failed
00003A95	E5D7D2E2 40404040			2724+	DC	CL8' VPKS'	instruction name
00003AA0	00003B18			2725+	DC	A(RE54)	address of v1 result
00003AA4	00003B28			2726+	DC	A(RE54+16)	address of v2 source
00003AA8	00003B38			2727+	DC	A(RE54+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00003AAC	00000010			2728+	DC	A(16)	result length	
00003AB0	00003B18			2729+REA54	DC	A(RE54)	result address	
00003AB8	00000000 00000000			2730+	DS	2FD	gap	
00003AC0	00000000 00000000							
00003AC8	00000000 00000000			2731+V1054	DS	XL16	V1 output	
00003AD0	00000000 00000000							
00003AD8	00000000 00000000			2732+	DS	2FD	gap	
00003AE0	00000000 00000000							
00003AE8				2733+*				
00003AE8	E310 5024 0014		00000024	2734+X54	DS	0F		
00003AEE	E761 0000 0806		00000000	2735+	LGF	R1, V2ADDR	load v2 source	
00003AF4	E310 5028 0014		00000028	2736+	VL	v22, 0(R1)	use v21 to test decoder	
00003AFA	E771 0000 0806		00000000	2737+	LGF	R1, V3ADDR	load v3 source	
00003B00	E756 7010 2E97			2738+	VL	v23, 0(R1)	use v22 to test decoder	
00003B06	B98D 0020			2739+	VPKS	V21, V22, V23, 2, 1	test instruction	
00003B0A	5020 500C		0000000C	2740+	EPSW	R2, R0	extract psw	
00003B0E	E750 5048 080E		00003AC8	2741+	ST	R2, CCPSW	to save CC	
00003B14	07FB			2742+	VST	V21, V1054	save v1 output	
00003B18				2743+	BR	R11	return	
00003B18				2744+RE54	DC	0F	V1 for this test	
00003B18	80008000 80008000			2745+	DROP	R5		
00003B20	80008000 80008000			2746	DC	XL16' 8000800080008000 8000800080008000'	result	
00003B28	F111F133 F155F177			2747	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v2	
00003B30	F199F1BB F1DDF1FF							
00003B38	F101F203 F405F607			2748	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v3	
00003B40	F809FAFB FCFDFE0F							
00003B48				2749				
00003B48				2750	VRR_B	VPKS, 2, 3		
00003B48		00003B48		2751+	DS	0FD		
00003B48	00003BB0			2752+	USING	*, R5	base for test data and test routine	
00003B4C	0037			2753+T55	DC	A(X55)	address of test routine	
00003B4E	00			2754+	DC	H' 55'	test number	
00003B4F	02			2755+	DC	X' 00'		
00003B50	01			2756+	DC	HL1' 2'	m4 used	
00003B51	03			2757+	DC	HL1' 1'	m5 used	
00003B52	0E			2758+	DC	HL1' 3'	CC	
00003B54	00000000 00000000			2759+	DC	HL1' 14'	CC failed mask	
00003B5C	FF			2760+	DS	2F	extracted PSW after test (has CC)	
00003B5D	E5D7D2E2 40404040			2761+	DC	X' FF'	extracted CC, if test failed	
00003B68	00003BE0			2762+	DC	CL8' VPKS'	instruction name	
00003B6C	00003BF0			2763+	DC	A(RE55)	address of v1 result	
00003B70	00003C00			2764+	DC	A(RE55+16)	address of v2 source	
00003B74	00000010			2765+	DC	A(RE55+32)	address of v3 source	
00003B78	00003BE0			2766+	DC	A(16)	result length	
00003B80	00000000 00000000			2767+REA55	DC	A(RE55)	result address	
00003B88	00000000 00000000			2768+	DS	2FD	gap	
00003B90	00000000 00000000			2769+V1055	DS	XL16	V1 output	
00003B98	00000000 00000000							
00003BA0	00000000 00000000			2770+	DS	2FD	gap	
00003BA8	00000000 00000000							
00003BB0				2771+*				
00003BB0	E310 5024 0014		00000024	2772+X55	DS	0F		
00003BB6	E761 0000 0806		00000000	2773+	LGF	R1, V2ADDR	load v2 source	
				2774+	VL	v22, 0(R1)	use v21 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00003BBC	E310 5028 0014		00000028	2775+	LGF	R1, V3ADDR	load v3 source	
00003BC2	E771 0000 0806		00000000	2776+	VL	v23, 0(R1)	use v22 to test decoder	
00003BC8	E756 7010 2E97			2777+	VPKS	V21, V22, V23, 2, 1	test instruction	
00003BCE	B98D 0020			2778+	EPSW	R2, R0	extract psw	
00003BD2	5020 500C		0000000C	2779+	ST	R2, CCPSW	to save CC	
00003BD6	E750 5048 080E		00003B90	2780+	VST	V21, V1055	save v1 output	
00003BDC	07FB			2781+	BR	R11	return	
00003BE0				2782+RE55	DC	0F	V1 for this test	
00003BE0				2783+	DROP	R5		
00003BE0	80008000 80008000			2784	DC	XL16' 8000800080008000 8000800080008000'	result t	
00003BE8	80008000 80008000							
00003BF0	F101F203 F405F607			2785	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v2	
00003BF8	F809FAFB FCFDFE0F							
00003C00	F111F133 F155F177			2786	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v3	
00003C08	F199F1BB F1DDF1FF							
				2787				
				2788	*Doubleword			
				2789	VRR_B	VPKS, 3, 0		
00003C10				2790+	DS	0FD		
00003C10		00003C10		2791+	USING	*, R5	base for test data and test routine	
00003C10	00003C78			2792+T56	DC	A(X56)	address of test routine	
00003C14	0038			2793+	DC	H' 56'	test number	
00003C16	00			2794+	DC	X' 00'		
00003C17	03			2795+	DC	HL1' 3'	m4 used	
00003C18	01			2796+	DC	HL1' 1'	m5 used	
00003C19	00			2797+	DC	HL1' 0'	CC	
00003C1A	07			2798+	DC	HL1' 7'	CC failed mask	
00003C1C	00000000 00000000			2799+	DS	2F	extracted PSW after test (has CC)	
00003C24	FF			2800+	DC	X' FF'	extracted CC, if test failed	
00003C25	E5D7D2E2 40404040			2801+	DC	CL8' VPKS'	instruction name	
00003C30	00003CA8			2802+	DC	A(RE56)	address of v1 result	
00003C34	00003CB8			2803+	DC	A(RE56+16)	address of v2 source	
00003C38	00003CC8			2804+	DC	A(RE56+32)	address of v3 source	
00003C3C	00000010			2805+	DC	A(16)	result length	
00003C40	00003CA8			2806+REA56	DC	A(RE56)	result address	
00003C48	00000000 00000000			2807+	DS	2FD	gap	
00003C50	00000000 00000000							
00003C58	00000000 00000000			2808+V1056	DS	XL16	V1 output	
00003C60	00000000 00000000							
00003C68	00000000 00000000			2809+	DS	2FD	gap	
00003C70	00000000 00000000							
				2810+*				
00003C78				2811+X56	DS	0F		
00003C78	E310 5024 0014		00000024	2812+	LGF	R1, V2ADDR	load v2 source	
00003C7E	E761 0000 0806		00000000	2813+	VL	v22, 0(R1)	use v21 to test decoder	
00003C84	E310 5028 0014		00000028	2814+	LGF	R1, V3ADDR	load v3 source	
00003C8A	E771 0000 0806		00000000	2815+	VL	v23, 0(R1)	use v22 to test decoder	
00003C90	E756 7010 3E97			2816+	VPKS	V21, V22, V23, 3, 1	test instruction	
00003C96	B98D 0020			2817+	EPSW	R2, R0	extract psw	
00003C9A	5020 500C		0000000C	2818+	ST	R2, CCPSW	to save CC	
00003C9E	E750 5048 080E		00003C58	2819+	VST	V21, V1056	save v1 output	
00003CA4	07FB			2820+	BR	R11	return	
00003CA8				2821+RE56	DC	0F	V1 for this test	
00003CA8				2822+	DROP	R5		
00003CA8	11335577 22446688			2823	DC	XL16' 1133557722446688 FEFDFCFBFAF9F8F7'	result t	
00003CB0	FEFDFCFB FAF9F8F7							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00003CB8	00000000	11335577		2824	DC	XL16'	0000000011335577 0000000022446688'	v2
00003CC0	00000000	22446688						
00003CC8	FFFFFFFF	FEFDFCFB		2825	DC	XL16'	FFFFFFFFFEFDFCFB FFFFFFFFAF9F8F7'	v3
00003CD0	FFFFFFFF	FAF9F8F7						
				2826				
00003CD8				2827	VRR_B	VPKS, 3, 0		
00003CD8				2828+	DS	OFD		
00003CD8	00003D40	00003CD8		2829+	USING	*, R5	base for test data and test routine	
00003CDC	0039			2830+T57	DC	A(X57)	address of test routine	
00003CDE	00			2831+	DC	H' 57'	test number	
00003CDF	03			2832+	DC	X' 00'		
00003CE0	01			2833+	DC	HL1' 3'	m4 used	
00003CE1	00			2834+	DC	HL1' 1'	m5 used	
00003CE2	07			2835+	DC	HL1' 0'	CC	
00003CE4	00000000	00000000		2836+	DC	HL1' 7'	CC failed mask	
00003CEC	FF			2837+	DS	2F	extracted PSW after test (has CC)	
00003CED	E5D7D2E2	40404040		2838+	DC	X' FF'	extracted CC, if test failed	
00003CF8	00003D70			2839+	DC	CL8' VPKS'	instruction name	
00003CFC	00003D80			2840+	DC	A(RE57)	address of v1 result	
00003D00	00003D90			2841+	DC	A(RE57+16)	address of v2 source	
00003D04	00000010			2842+	DC	A(RE57+32)	address of v3 source	
00003D08	00003D70			2843+	DC	A(16)	result length	
00003D10	00000000	00000000		2844+REA57	DC	A(RE57)	result address	
00003D18	00000000	00000000		2845+	DS	2FD	gap	
00003D20	00000000	00000000		2846+V1057	DS	XL16	V1 output	
00003D28	00000000	00000000						
00003D30	00000000	00000000		2847+	DS	2FD	gap	
00003D38	00000000	00000000						
				2848+*				
00003D40				2849+X57	DS	0F		
00003D40	E310 5024 0014		00000024	2850+	LGF	R1, V2ADDR	load v2 source	
00003D46	E761 0000 0806		00000000	2851+	VL	v22, 0(R1)	use v21 to test decoder	
00003D4C	E310 5028 0014		00000028	2852+	LGF	R1, V3ADDR	load v3 source	
00003D52	E771 0000 0806		00000000	2853+	VL	v23, 0(R1)	use v22 to test decoder	
00003D58	E756 7010 3E97			2854+	VPKS	V21, V22, V23, 3, 1	test instruction	
00003D5E	B98D 0020			2855+	EPSW	R2, R0	extract psw	
00003D62	5020 500C		0000000C	2856+	ST	R2, CCPSW	to save CC	
00003D66	E750 5048 080E		00003D20	2857+	VST	V21, V1057	save v1 output	
00003D6C	07FB			2858+	BR	R11	return	
00003D70				2859+RE57	DC	0F	V1 for this test	
00003D70				2860+	DROP	R5		
00003D70	FEFDFCFB FAF9F8F7			2861	DC	XL16' FEFDFCFBFAF9F8F7 1133557722446688 '	result t	
00003D78	11335577 22446688							
00003D80	FFFFFFFF	FEFDFCFB		2862	DC	XL16' FFFFFFFFFEFDFCFB FFFFFFFFAF9F8F7'	v2	
00003D88	FFFFFFFF	FAF9F8F7						
00003D90	00000000	11335577		2863	DC	XL16' 0000000011335577 0000000022446688'	v3	
00003D98	00000000	22446688						
				2864				
00003DA0				2865	VRR_B	VPKS, 3, 1		
00003DA0			00003DA0	2866+	DS	OFD		
00003DA0	00003E08			2867+	USING	*, R5	base for test data and test routine	
00003DA4	003A			2868+T58	DC	A(X58)	address of test routine	
00003DA6	00			2869+	DC	H' 58'	test number	
00003DA7	03			2870+	DC	X' 00'		
				2871+	DC	HL1' 3'	m4 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00003DA8	01			2872+	DC	HL1' 1' m5 used
00003DA9	01			2873+	DC	HL1' 1' CC
00003DAA	0B			2874+	DC	HL1' 11' CC failed mask
00003DAC	00000000	00000000		2875+	DS	2F extracted PSW after test (has CC)
00003DB4	FF			2876+	DC	X' FF' extracted CC, if test failed
00003DB5	E5D7D2E2	40404040		2877+	DC	CL8' VPKS' instruction name
00003DC0	00003E38			2878+	DC	A(RE58) address of v1 result
00003DC4	00003E48			2879+	DC	A(RE58+16) address of v2 source
00003DC8	00003E58			2880+	DC	A(RE58+32) address of v3 source
00003DCC	00000010			2881+	DC	A(16) result length
00003DD0	00003E38			2882+REA58	DC	A(RE58) result address
00003DD8	00000000	00000000		2883+	DS	2FD gap
00003DE0	00000000	00000000				
00003DE8	00000000	00000000		2884+V1058	DS	XL16 V1 output
00003DF0	00000000	00000000				
00003DF8	00000000	00000000		2885+	DS	2FD gap
00003E00	00000000	00000000				
00003E08				2886+*		
00003E08	E310 5024 0014		00000024	2887+X58	DS	0F
00003E0E	E761 0000 0806		00000000	2888+	LGF	R1, V2ADDR load v2 source
00003E14	E310 5028 0014		00000028	2889+	VL	v22, 0(R1) use v21 to test decoder
00003E1A	E771 0000 0806		00000000	2890+	LGF	R1, V3ADDR load v3 source
00003E20	E756 7010 3E97			2891+	VL	v23, 0(R1) use v22 to test decoder
00003E26	B98D 0020			2892+	VPKS	V21, V22, V23, 3, 1 test instruction
00003E2A	5020 500C		0000000C	2893+	EPSW	R2, R0 extract psw
00003E2E	E750 5048 080E		00003DE8	2894+	ST	R2, CCPSW to save CC
00003E34	07FB			2895+	VST	V21, V1058 save v1 output
00003E38				2896+	BR	R11 return
00003E38				2897+RE58	DC	0F V1 for this test
00003E38				2898+	DROP	R5
00003E38	12030405 7FFFFFFF			2899	DC	XL16' 120304057FFFFFFF 1133557719BB2DFF' result t
00003E40	11335577 19BB2DFF					
00003E48	00000000 12030405			2900	DC	XL16' 0000000012030405 08090A0B0C0D0E0F' v2
00003E50	08090A0B 0C0D0E0F					
00003E58	00000000 11335577			2901	DC	XL16' 0000000011335577 0000000019BB2DFF' v3
00003E60	00000000 19BB2DFF					
00003E68				2902		
00003E68				2903	VRR_B	VPKS, 3, 1
00003E68	00003ED0	00003E68		2904+	DS	0FD
00003E6C	003B			2905+	USING	*, R5 base for test data and test routine
00003E6E	00			2906+T59	DC	A(X59) address of test routine
00003E6F	03			2907+	DC	H' 59' test number
00003E70	01			2908+	DC	X' 00'
00003E71	01			2909+	DC	HL1' 3' m4 used
00003E72	0B			2910+	DC	HL1' 1' m5 used
00003E74	00000000	00000000		2911+	DC	HL1' 1' CC
00003E7C	FF			2912+	DC	HL1' 11' CC failed mask
00003E7D	E5D7D2E2	40404040		2913+	DS	2F extracted PSW after test (has CC)
00003E88	00003F00			2914+	DC	X' FF' extracted CC, if test failed
00003E8C	00003F10			2915+	DC	CL8' VPKS' instruction name
00003E90	00003F20			2916+	DC	A(RE59) address of v1 result
00003E94	00000010			2917+	DC	A(RE59+16) address of v2 source
00003E98	00003F00			2918+	DC	A(RE59+32) address of v3 source
00003EA0	00000000	00000000		2919+	DC	A(16) result length
				2920+REA59	DC	A(RE59) result address
				2921+	DS	2FD gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003EA8	00000000	00000000					
00003EB0	00000000	00000000		2922+V1059	DS	XL16	V1 output
00003EB8	00000000	00000000					
00003EC0	00000000	00000000		2923+	DS	2FD	gap
00003EC8	00000000	00000000					
00003ED0				2924+*			
00003ED0	E310 5024 0014		00000024	2925+X59	DS	0F	
00003ED6	E761 0000 0806		00000000	2926+	LGF	R1, V2ADDR	load v2 source
00003EDC	E310 5028 0014		00000028	2927+	VL	v22, 0(R1)	use v21 to test decoder
00003EE2	E771 0000 0806		00000000	2928+	LGF	R1, V3ADDR	load v3 source
00003EE8	E756 7010 3E97		00000000	2929+	VL	v23, 0(R1)	use v22 to test decoder
00003EEE	B98D 0020			2930+	VPKS	V21, V22, V23, 3, 1	test instruction
00003EE8	B98D 0020			2931+	EPSW	R2, R0	extract psw
00003EF2	5020 500C		0000000C	2932+	ST	R2, CCPSW	to save CC
00003EF6	E750 5048 080E		00003EB0	2933+	VST	V21, V1059	save v1 output
00003EFC	07FB			2934+	BR	R11	return
00003F00				2935+RE59	DC	0F	V1 for this test
00003F00				2936+	DROP	R5	
00003F00	11335577 19BB2DFF			2937	DC	XL16' 1133557719BB2DFF 120304057FFFFFFF'	result
00003F08	12030405 7FFFFFFF						
00003F10	00000000 11335577			2938	DC	XL16' 0000000011335577 0000000019BB2DFF'	v2
00003F18	00000000 19BB2DFF						
00003F20	00000000 12030405			2939	DC	XL16' 0000000012030405 08090A0B0C0D0E0F'	v3
00003F28	08090A0B 0C0D0E0F						
00003F30				2940			
00003F30				2941	VRR_B	VPKS, 3, 3	
00003F30	00003F98	00003F30		2942+	DS	0FD	
00003F34	003C			2943+	USING	*, R5	base for test data and test routine
00003F36	00			2944+T60	DC	A(X60)	address of test routine
00003F37	03			2945+	DC	H' 60'	test number
00003F38	01			2946+	DC	X' 00'	
00003F39	03			2947+	DC	HL1' 3'	m4 used
00003F3A	0E			2948+	DC	HL1' 1'	m5 used
00003F3C	00000000 00000000			2949+	DC	HL1' 3'	CC
00003F44	FF			2950+	DC	HL1' 14'	CC failed mask
00003F45	E5D7D2E2 40404040			2951+	DS	2F	extracted PSW after test (has CC)
00003F50	00003FC8			2952+	DC	X' FF'	extracted CC, if test failed
00003F54	00003FD8			2953+	DC	CL8' VPKS'	instruction name
00003F58	00003FE8			2954+	DC	A(RE60)	address of v1 result
00003F5C	00000010			2955+	DC	A(RE60+16)	address of v2 source
00003F60	00003FC8			2956+	DC	A(RE60+32)	address of v3 source
00003F68	00000000 00000000			2957+	DC	A(16)	result length
00003F70	00000000 00000000			2958+REA60	DC	A(RE60)	result address
00003F78	00000000 00000000			2959+	DS	2FD	gap
00003F80	00000000 00000000						
00003F88	00000000 00000000			2960+V1060	DS	XL16	V1 output
00003F90	00000000 00000000						
00003F98				2961+	DS	2FD	gap
00003F98				2962+*			
00003F98	E310 5024 0014		00000024	2963+X60	DS	0F	
00003F9E	E761 0000 0806		00000000	2964+	LGF	R1, V2ADDR	load v2 source
00003FA4	E310 5028 0014		00000028	2965+	VL	v22, 0(R1)	use v21 to test decoder
00003FAA	E771 0000 0806		00000000	2966+	LGF	R1, V3ADDR	load v3 source
00003FB0	E756 7010 3E97			2967+	VL	v23, 0(R1)	use v22 to test decoder
				2968+	VPKS	V21, V22, V23, 3, 1	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003FB6	B98D 0020			2969+	EPSW	R2, R0	extract psw
00003FBA	5020 500C		0000000C	2970+	ST	R2, CCPSW	to save CC
00003FBE	E750 5048 080E		00003F78	2971+	VST	V21, V1060	save v1 output
00003FC4	07FB			2972+	BR	R11	return
00003FC8				2973+RE60	DC	0F	V1 for this test
00003FC8				2974+	DROP	R5	
00003FC8	7FFFFFFF 7FFFFFFF			2975	DC	XL16' 7FFFFFFF7FFFFFFF 7FFFFFFF7FFFFFFF'	result
00003FD0	7FFFFFFF 7FFFFFFF						
00003FD8	01110133 01550177			2976	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00003FE0	019901BB 01DD01FF						
00003FE8	01010203 04050607			2977	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v3
00003FF0	08090A0B 0C0D0E0F						
				2978			
				2979	VRR_B	VPKS, 3, 3	
00003FF8				2980+	DS	0FD	
00003FF8		00003FF8		2981+	USING	*, R5	base for test data and test routine
00003FF8	00004060			2982+T61	DC	A(X61)	address of test routine
00003FFC	003D			2983+	DC	H' 61'	test number
00003FFE	00			2984+	DC	X' 00'	
00003FFF	03			2985+	DC	HL1' 3'	m4 used
00004000	01			2986+	DC	HL1' 1'	m5 used
00004001	03			2987+	DC	HL1' 3'	CC
00004002	0E			2988+	DC	HL1' 14'	CC failed mask
00004004	00000000 00000000			2989+	DS	2F	extracted PSW after test (has CC)
0000400C	FF			2990+	DC	X' FF'	extracted CC, if test failed
0000400D	E5D7D2E2 40404040			2991+	DC	CL8' VPKS'	instruction name
00004018	00004090			2992+	DC	A(RE61)	address of v1 result
0000401C	000040A0			2993+	DC	A(RE61+16)	address of v2 source
00004020	000040B0			2994+	DC	A(RE61+32)	address of v3 source
00004024	00000010			2995+	DC	A(16)	result length
00004028	00004090			2996+REA61	DC	A(RE61)	result address
00004030	00000000 00000000			2997+	DS	2FD	gap
00004038	00000000 00000000						
00004040	00000000 00000000			2998+V1061	DS	XL16	V1 output
00004048	00000000 00000000						
00004050	00000000 00000000			2999+	DS	2FD	gap
00004058	00000000 00000000						
				3000+*			
00004060				3001+X61	DS	0F	
00004060	E310 5024 0014		00000024	3002+	LGF	R1, V2ADDR	load v2 source
00004066	E761 0000 0806		00000000	3003+	VL	v22, 0(R1)	use v21 to test decoder
0000406C	E310 5028 0014		00000028	3004+	LGF	R1, V3ADDR	load v3 source
00004072	E771 0000 0806		00000000	3005+	VL	v23, 0(R1)	use v22 to test decoder
00004078	E756 7010 3E97			3006+	VPKS	V21, V22, V23, 3, 1	test instruction
0000407E	B98D 0020			3007+	EPSW	R2, R0	extract psw
00004082	5020 500C		0000000C	3008+	ST	R2, CCPSW	to save CC
00004086	E750 5048 080E		00004040	3009+	VST	V21, V1061	save v1 output
0000408C	07FB			3010+	BR	R11	return
00004090				3011+RE61	DC	0F	V1 for this test
00004090				3012+	DROP	R5	
00004090	7FFFFFFF 7FFFFFFF			3013	DC	XL16' 7FFFFFFF7FFFFFFF 7FFFFFFF7FFFFFFF'	result
00004098	7FFFFFFF 7FFFFFFF						
000040A0	01010203 04050607			3014	DC	XL16' 0101020304050607 08090A0B0C0D0E0F'	v2
000040A8	08090A0B 0C0D0E0F						
000040B0	01110133 01550177			3015	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
000040B8	019901BB 01DD01FF						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				3016			
				3017	VRR_B	VPKS, 3, 3	
000040C0				3018+	DS	0FD	
000040C0		000040C0		3019+	USING	*, R5	base for test data and test routine
000040C0	00004128			3020+T62	DC	A(X62)	address of test routine
000040C4	003E			3021+	DC	H' 62'	test number
000040C6	00			3022+	DC	X' 00'	
000040C7	03			3023+	DC	HL1' 3'	m4 used
000040C8	01			3024+	DC	HL1' 1'	m5 used
000040C9	03			3025+	DC	HL1' 3'	CC
000040CA	0E			3026+	DC	HL1' 14'	CC failed mask
000040CC	00000000 00000000			3027+	DS	2F	extracted PSW after test (has CC)
000040D4	FF			3028+	DC	X' FF'	extracted CC, if test failed
000040D5	E5D7D2E2 40404040			3029+	DC	CL8' VPKS'	instruction name
000040E0	00004158			3030+	DC	A(RE62)	address of v1 result
000040E4	00004168			3031+	DC	A(RE62+16)	address of v2 source
000040E8	00004178			3032+	DC	A(RE62+32)	address of v3 source
000040EC	00000010			3033+	DC	A(16)	result length
000040F0	00004158			3034+REA62	DC	A(RE62)	result address
000040F8	00000000 00000000			3035+	DS	2FD	gap
00004100	00000000 00000000						
00004108	00000000 00000000			3036+V1062	DS	XL16	V1 output
00004110	00000000 00000000						
00004118	00000000 00000000			3037+	DS	2FD	gap
00004120	00000000 00000000						
				3038+*			
00004128				3039+X62	DS	0F	
00004128	E310 5024 0014		00000024	3040+	LGF	R1, V2ADDR	load v2 source
0000412E	E761 0000 0806		00000000	3041+	VL	v22, 0(R1)	use v21 to test decoder
00004134	E310 5028 0014		00000028	3042+	LGF	R1, V3ADDR	load v3 source
0000413A	E771 0000 0806		00000000	3043+	VL	v23, 0(R1)	use v22 to test decoder
00004140	E756 7010 3E97			3044+	VPKS	V21, V22, V23, 3, 1	test instruction
00004146	B98D 0020			3045+	EPSW	R2, R0	extract psw
0000414A	5020 500C		0000000C	3046+	ST	R2, CCPSW	to save CC
0000414E	E750 5048 080E		00004108	3047+	VST	V21, V1062	save v1 output
00004154	07FB			3048+	BR	R11	return
00004158				3049+RE62	DC	0F	V1 for this test
00004158				3050+	DROP	R5	
00004158	80000000 80000000			3051	DC	XL16' 8000000080000000 8000000080000000'	result t
00004160	80000000 80000000						
00004168	F111F133 F155F177			3052	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v2
00004170	F199F1BB F1DDF1FF						
00004178	F101F203 F405F607			3053	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v3
00004180	F809FAFB FCFDFE0F						
				3054			
00004188				3055	VRR_B	VPKS, 3, 3	
00004188		00004188		3056+	DS	0FD	
00004188	000041F0			3057+	USING	*, R5	base for test data and test routine
0000418C	003F			3058+T63	DC	A(X63)	address of test routine
0000418E	00			3059+	DC	H' 63'	test number
0000418F	00			3060+	DC	X' 00'	
0000418F	03			3061+	DC	HL1' 3'	m4 used
00004190	01			3062+	DC	HL1' 1'	m5 used
00004191	03			3063+	DC	HL1' 3'	CC
00004192	0E			3064+	DC	HL1' 14'	CC failed mask
00004194	00000000 00000000			3065+	DS	2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000419C	FF			3066+	DC	X' FF'	extracted CC, if test failed
0000419D	E5D7D2E2 40404040			3067+	DC	CL8' VPKS'	instruction name
000041A8	00004220			3068+	DC	A(RE63)	address of v1 result
000041AC	00004230			3069+	DC	A(RE63+16)	address of v2 source
000041B0	00004240			3070+	DC	A(RE63+32)	address of v3 source
000041B4	00000010			3071+	DC	A(16)	result length
000041B8	00004220			3072+REA63	DC	A(RE63)	result address
000041C0	00000000 00000000			3073+	DS	2FD	gap
000041C8	00000000 00000000						
000041D0	00000000 00000000			3074+V1063	DS	XL16	V1 output
000041D8	00000000 00000000						
000041E0	00000000 00000000			3075+	DS	2FD	gap
000041E8	00000000 00000000						
				3076+*			
000041F0				3077+X63	DS	0F	
000041F0	E310 5024 0014		00000024	3078+	LGF	R1, V2ADDR	load v2 source
000041F6	E761 0000 0806		00000000	3079+	VL	v22, 0(R1)	use v21 to test decoder
000041FC	E310 5028 0014		00000028	3080+	LGF	R1, V3ADDR	load v3 source
00004202	E771 0000 0806		00000000	3081+	VL	v23, 0(R1)	use v22 to test decoder
00004208	E756 7010 3E97			3082+	VPKS	V21, V22, V23, 3, 1	test instruction
0000420E	B98D 0020			3083+	EPSW	R2, R0	extract psw
00004212	5020 500C		0000000C	3084+	ST	R2, CCPSW	to save CC
00004216	E750 5048 080E		000041D0	3085+	VST	V21, V1063	save v1 output
0000421C	07FB			3086+	BR	R11	return
00004220				3087+RE63	DC	0F	V1 for this test
00004220				3088+	DROP	R5	
00004220	80000000 80000000			3089	DC	XL16' 8000000080000000 8000000080000000'	result t
00004228	80000000 80000000						
00004230	F101F203 F405F607			3090	DC	XL16' F101F203F405F607 F809FAFBFCFDFE0F'	v2
00004238	F809FAFB FCFDFE0F						
00004240	F111F133 F155F177			3091	DC	XL16' F111F133F155F177 F199F1BBF1DDF1FF'	v3
00004248	F199F1BB F1DDF1FF						
				3092			
				3093 *			
				3094 * m4 sc. . .			
				3095 *			
				3096	VRR_B	VPKS, 1, 0	
00004250				3097+	DS	0FD	
00004250		00004250		3098+	USING	*, R5	base for test data and test routine
00004250	000042B8			3099+T64	DC	A(X64)	address of test routine
00004254	0040			3100+	DC	H' 64'	test number
00004256	00			3101+	DC	X' 00'	
00004257	01			3102+	DC	HL1' 1'	m4 used
00004258	01			3103+	DC	HL1' 1'	m5 used
00004259	00			3104+	DC	HL1' 0'	CC
0000425A	07			3105+	DC	HL1' 7'	CC failed mask
0000425C	00000000 00000000			3106+	DS	2F	extracted PSW after test (has CC)
00004264	FF			3107+	DC	X' FF'	extracted CC, if test failed
00004265	E5D7D2E2 40404040			3108+	DC	CL8' VPKS'	instruction name
00004270	000042E8			3109+	DC	A(RE64)	address of v1 result
00004274	000042F8			3110+	DC	A(RE64+16)	address of v2 source
00004278	00004308			3111+	DC	A(RE64+32)	address of v3 source
0000427C	00000010			3112+	DC	A(16)	result length
00004280	000042E8			3113+REA64	DC	A(RE64)	result address
00004288	00000000 00000000			3114+	DS	2FD	gap
00004290	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
00004298	00000000 00000000			3115+V1064	DS	XL16		V1 output	
000042A0	00000000 00000000								
000042A8	00000000 00000000			3116+	DS	2FD		gap	
000042B0	00000000 00000000								
				3117+*					
000042B8				3118+X64	DS	0F			
000042B8	E310 5024 0014		00000024	3119+	LGF	R1, V2ADDR		load v2 source	
000042BE	E761 0000 0806		00000000	3120+	VL	v22, 0(R1)		use v21 to test decoder	
000042C4	E310 5028 0014		00000028	3121+	LGF	R1, V3ADDR		load v3 source	
000042CA	E771 0000 0806		00000000	3122+	VL	v23, 0(R1)		use v22 to test decoder	
000042D0	E756 7010 1E97			3123+	VPKS	V21, V22, V23, 1, 1		test instruction	
000042D6	B98D 0020			3124+	EPSW	R2, R0		extract psw	
000042DA	5020 500C		0000000C	3125+	ST	R2, CCPSW		to save CC	
000042DE	E750 5048 080E		00004298	3126+	VST	V21, V1064		save v1 output	
000042E4	07FB			3127+	BR	R11		return	
000042E8				3128+RE64	DC	0F		V1 for this test	
000042E8				3129+	DROP	R5			
000042E8	51535557 595B5D5F			3130	DC	XL16' 51535557 595B5D5F 61636567 696B6D6F'		result	
000042F0	61636567 696B6D6F								
000042F8	00510053 00550057			3131	DC	XL16' 00510053 00550057 0059005B 005D005F'		v2	
00004300	0059005B 005D005F								
00004308	00610063 00650067			3132	DC	XL16' 00610063 00650067 0069006B 006D006F'		v3	
00004310	0069006B 006D006F								
				3133					
				3134	VRR_B	VPKS, 2, 0			
00004318				3135+	DS	0FD			
00004318		00004318		3136+	USING	*, R5		base for test data and test routine	
00004318	00004380			3137+T65	DC	A(X65)		address of test routine	
0000431C	0041			3138+	DC	H' 65'		test number	
0000431E	00			3139+	DC	X' 00'			
0000431F	02			3140+	DC	HL1' 2'		m4 used	
00004320	01			3141+	DC	HL1' 1'		m5 used	
00004321	00			3142+	DC	HL1' 0'		CC	
00004322	07			3143+	DC	HL1' 7'		CC failed mask	
00004324	00000000 00000000			3144+	DS	2F		extracted PSW after test (has CC)	
0000432C	FF			3145+	DC	X' FF'		extracted CC, if test failed	
0000432D	E5D7D2E2 40404040			3146+	DC	CL8' VPKS'		instruction name	
00004338	000043B0			3147+	DC	A(RE65)		address of v1 result	
0000433C	000043C0			3148+	DC	A(RE65+16)		address of v2 source	
00004340	000043D0			3149+	DC	A(RE65+32)		address of v3 source	
00004344	00000010			3150+	DC	A(16)		result length	
00004348	000043B0			3151+REA65	DC	A(RE65)		result address	
00004350	00000000 00000000			3152+	DS	2FD		gap	
00004358	00000000 00000000								
00004360	00000000 00000000			3153+V1065	DS	XL16		V1 output	
00004368	00000000 00000000								
00004370	00000000 00000000			3154+	DS	2FD		gap	
00004378	00000000 00000000								
				3155+*					
00004380				3156+X65	DS	0F			
00004380	E310 5024 0014		00000024	3157+	LGF	R1, V2ADDR		load v2 source	
00004386	E761 0000 0806		00000000	3158+	VL	v22, 0(R1)		use v21 to test decoder	
0000438C	E310 5028 0014		00000028	3159+	LGF	R1, V3ADDR		load v3 source	
00004392	E771 0000 0806		00000000	3160+	VL	v23, 0(R1)		use v22 to test decoder	
00004398	E756 7010 2E97			3161+	VPKS	V21, V22, V23, 2, 1		test instruction	
0000439E	B98D 0020			3162+	EPSW	R2, R0		extract psw	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000043A2	5020 500C		0000000C	3163+	ST	R2, CCPSW		to save CC	
000043A6	E750 5048 080E		00004360	3164+	VST	V21, V1065		save v1 output	
000043AC	07FB			3165+	BR	R11		return	
000043B0				3166+RE65	DC	0F		V1 for this test	
000043B0				3167+	DROP	R5			
000043B0	52535657 5A5B5E5F			3168	DC	XL16' 52535657 5A5B5E5F 62636667 6A6B6E6F'		result t	
000043B8	62636667 6A6B6E6F								
000043C0	00005253 00005657			3169	DC	XL16' 00005253 00005657 00005A5B 00005E5F'		v2	
000043C8	00005A5B 00005E5F								
000043D0	00006263 00006667			3170	DC	XL16' 00006263 00006667 00006A6B 00006E6F'		v3	
000043D8	00006A6B 00006E6F								
000043E0				3171					
000043E0		000043E0		3172	VRR_B	VPKS, 3, 0			
000043E0	00004448			3173+	DS	0FD			
000043E4	0042			3174+	USING	*, R5		base for test data and test routine	
000043E6	00			3175+T66	DC	A(X66)		address of test routine	
000043E7	03			3176+	DC	H' 66'		test number	
000043E8	01			3177+	DC	X' 00'			
000043E9	00			3178+	DC	HL1' 3'		m4 used	
000043EA	07			3179+	DC	HL1' 1'		m5 used	
000043EC	00000000 00000000			3180+	DC	HL1' 0'		CC	
000043F4	FF			3181+	DC	HL1' 7'		CC failed mask	
000043F5	E5D7D2E2 40404040			3182+	DS	2F		extracted PSW after test (has CC)	
00004400	00004478			3183+	DC	X' FF'		extracted CC, if test failed	
00004404	00004488			3184+	DC	CL8' VPKS'		instruction name	
00004408	00004498			3185+	DC	A(RE66)		address of v1 result	
0000440C	00000010			3186+	DC	A(RE66+16)		address of v2 source	
00004410	00004478			3187+	DC	A(RE66+32)		address of v3 source	
00004418	00000000 00000000			3188+	DC	A(16)		result length	
00004420	00000000 00000000			3189+REA66	DC	A(RE66)		result address	
00004428	00000000 00000000			3190+	DS	2FD		gap	
00004430	00000000 00000000			3191+V1066	DS	XL16		V1 output	
00004438	00000000 00000000			3192+	DS	2FD		gap	
00004440	00000000 00000000								
00004448				3193+*					
00004448	E310 5024 0014		00000024	3194+X66	DS	0F			
0000444E	E761 0000 0806		00000000	3195+	LGF	R1, V2ADDR		load v2 source	
00004454	E310 5028 0014		00000028	3196+	VL	v22, 0(R1)		use v21 to test decoder	
0000445A	E771 0000 0806		00000000	3197+	LGF	R1, V3ADDR		load v3 source	
00004460	E756 7010 3E97			3198+	VL	v23, 0(R1)		use v22 to test decoder	
00004466	B98D 0020			3199+	VPKS	V21, V22, V23, 3, 1		test instruction	
0000446A	5020 500C		0000000C	3200+	EPSW	R2, R0		extract psw	
0000446E	E750 5048 080E		00004428	3201+	ST	R2, CCPSW		to save CC	
00004474	07FB			3202+	VST	V21, V1066		save v1 output	
00004478				3203+	BR	R11		return	
00004478				3204+RE66	DC	0F		V1 for this test	
00004478				3205+	DROP	R5			
00004478	54555657 5C5D5E5F			3206	DC	XL16' 54555657 5C5D5E5F 64656667 6C6D6E6F'		result t	
00004480	64656667 6C6D6E6F								
00004488	00000000 54555657			3207	DC	XL16' 00000000 54555657 00000000 5C5D5E5F'		v2	
00004490	00000000 5C5D5E5F								
00004498	00000000 64656667			3208	DC	XL16' 00000000 64656667 00000000 6C6D6E6F'		v3	
000044A0	00000000 6C6D6E6F								
				3209					

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				3210 *	-----
				3211 * VCEQ	- Vector Compare Equal
				3212 *	-----
				3213 *	cc=0: All elements equal
				3214 *	cc=1: At least one, but not all elements equal
				3215 *	cc=3: No element equal
				3216 *	-----
				3217 *	case - simple cc debug
				3218 *	-----
				3219 *	Byte
				3220	VRR_B VCEQ, 0, 0
000044A8				3221+	DS OFD
000044A8		000044A8		3222+	USING *, R5
000044A8	00004510			3223+T67	DC A(X67)
000044AC	0043			3224+	DC H' 67'
000044AE	00			3225+	DC X' 00'
000044AF	00			3226+	DC HL1' 0'
000044B0	01			3227+	DC HL1' 1'
000044B1	00			3228+	DC HL1' 0'
000044B2	07			3229+	DC HL1' 7'
000044B4	00000000	00000000		3230+	DS 2F
000044BC	FF			3231+	DC X' FF'
000044BD	E5C3C5D8	40404040		3232+	DC CL8' VCEQ'
000044C8	00004540			3233+	DC A(RE67)
000044CC	00004550			3234+	DC A(RE67+16)
000044D0	00004560			3235+	DC A(RE67+32)
000044D4	00000010			3236+	DC A(16)
000044D8	00004540			3237+REA67	DC A(RE67)
000044E0	00000000	00000000		3238+	DS 2FD
000044E8	00000000	00000000			
000044F0	00000000	00000000		3239+V1067	DS XL16
000044F8	00000000	00000000			
00004500	00000000	00000000		3240+	DS 2FD
00004508	00000000	00000000			
				3241+*	
00004510				3242+X67	DS OF
00004510	E310 5024 0014		00000024	3243+	LGF R1, V2ADDR
00004516	E761 0000 0806		00000000	3244+	VL v22, 0(R1)
0000451C	E310 5028 0014		00000028	3245+	LGF R1, V3ADDR
00004522	E771 0000 0806		00000000	3246+	VL v23, 0(R1)
00004528	E756 7010 0EF8			3247+	VCEQ V21, V22, V23, 0, 1
0000452E	B98D 0020			3248+	EPSW R2, R0
00004532	5020 500C		0000000C	3249+	ST R2, CCPSW
00004536	E750 5048 080E		000044F0	3250+	VST V21, V1067
0000453C	07FB			3251+	BR R11
00004540				3252+RE67	DC OF
00004540				3253+	DROP R5
00004540	FFFFFFFF FFFFFFFF			3254	DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'
00004548	FFFFFFFF FFFFFFFF				
00004550	00000000 00000000			3255	DC XL16' 0000000000000000 0000000000000000'
00004558	00000000 00000000				
00004560	00000000 00000000			3256	DC XL16' 0000000000000000 0000000000000000'
00004568	00000000 00000000				
				3257	
				3258	VRR_B VCEQ, 0, 1
00004570				3259+	DS OFD

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00004570		00004570		3260+	USING *, R5	base for test data and test routine
00004570	000045D8			3261+T68	DC A(X68)	address of test routine
00004574	0044			3262+	DC H' 68'	test number
00004576	00			3263+	DC X' 00'	
00004577	00			3264+	DC HL1' 0'	m4 used
00004578	01			3265+	DC HL1' 1'	m5 used
00004579	01			3266+	DC HL1' 1'	CC
0000457A	0B			3267+	DC HL1' 11'	CC failed mask
0000457C	00000000 00000000			3268+	DS 2F	extracted PSW after test (has CC)
00004584	FF			3269+	DC X' FF'	extracted CC, if test failed
00004585	E5C3C5D8 40404040			3270+	DC CL8' VCEQ'	instruction name
00004590	00004608			3271+	DC A(RE68)	address of v1 result
00004594	00004618			3272+	DC A(RE68+16)	address of v2 source
00004598	00004628			3273+	DC A(RE68+32)	address of v3 source
0000459C	00000010			3274+	DC A(16)	result length
000045A0	00004608			3275+REA68	DC A(RE68)	result address
000045A8	00000000 00000000			3276+	DS 2FD	gap
000045B0	00000000 00000000					
000045B8	00000000 00000000			3277+V1068	DS XL16	V1 output
000045C0	00000000 00000000					
000045C8	00000000 00000000			3278+	DS 2FD	gap
000045D0	00000000 00000000					
				3279+*		
000045D8				3280+X68	DS 0F	
000045D8	E310 5024 0014	00000024		3281+	LGF R1, V2ADDR	load v2 source
000045DE	E761 0000 0806	00000000		3282+	VL v22, 0(R1)	use v21 to test decoder
000045E4	E310 5028 0014	00000028		3283+	LGF R1, V3ADDR	load v3 source
000045EA	E771 0000 0806	00000000		3284+	VL v23, 0(R1)	use v22 to test decoder
000045F0	E756 7010 0EF8			3285+	VCEQ V21, V22, V23, 0, 1	test instruction
000045F6	B98D 0020			3286+	EPSW R2, R0	extract psw
000045FA	5020 500C	0000000C		3287+	ST R2, CCPSW	to save CC
000045FE	E750 5048 080E	000045B8		3288+	VST V21, V1068	save v1 output
00004604	07FB			3289+	BR R11	return
00004608				3290+RE68	DC 0F	V1 for this test
00004608				3291+	DROP R5	
00004608	FFFFFFFF FFFFFFFF			3292	DC XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result
00004610	00000000 FFFFFFFF					
00004618	00000000 00000000			3293	DC XL16' 0000000000000000 0000000000000000'	v2
00004620	00000000 00000000					
00004628	00000000 00000000			3294	DC XL16' 0000000000000000 8FFF8FFF00000000'	v3
00004630	8FFF8FFF 00000000					
				3295		
				3296	VRR_B VCEQ, 0, 3	
00004638				3297+	DS 0FD	
00004638		00004638		3298+	USING *, R5	base for test data and test routine
00004638	000046A0			3299+T69	DC A(X69)	address of test routine
0000463C	0045			3300+	DC H' 69'	test number
0000463E	00			3301+	DC X' 00'	
0000463F	00			3302+	DC HL1' 0'	m4 used
00004640	01			3303+	DC HL1' 1'	m5 used
00004641	03			3304+	DC HL1' 3'	CC
00004642	0E			3305+	DC HL1' 14'	CC failed mask
00004644	00000000 00000000			3306+	DS 2F	extracted PSW after test (has CC)
0000464C	FF			3307+	DC X' FF'	extracted CC, if test failed
0000464D	E5C3C5D8 40404040			3308+	DC CL8' VCEQ'	instruction name
00004658	000046D0			3309+	DC A(RE69)	address of v1 result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000465C	000046E0			3310+	DC	A(RE69+16)	address of v2 source
00004660	000046F0			3311+	DC	A(RE69+32)	address of v3 source
00004664	00000010			3312+	DC	A(16)	result length
00004668	000046D0			3313+REA69	DC	A(RE69)	result address
00004670	00000000 00000000			3314+	DS	2FD	gap
00004678	00000000 00000000						
00004680	00000000 00000000			3315+V1069	DS	XL16	V1 output
00004688	00000000 00000000						
00004690	00000000 00000000			3316+	DS	2FD	gap
00004698	00000000 00000000						
				3317+*			
000046A0				3318+X69	DS	0F	
000046A0	E310 5024 0014		00000024	3319+	LGF	R1, V2ADDR	load v2 source
000046A6	E761 0000 0806		00000000	3320+	VL	v22, 0(R1)	use v21 to test decoder
000046AC	E310 5028 0014		00000028	3321+	LGF	R1, V3ADDR	load v3 source
000046B2	E771 0000 0806		00000000	3322+	VL	v23, 0(R1)	use v22 to test decoder
000046B8	E756 7010 0EF8			3323+	VCEQ	V21, V22, V23, 0, 1	test instruction
000046BE	B98D 0020			3324+	EPSW	R2, R0	extract psw
000046C2	5020 500C		0000000C	3325+	ST	R2, CCPSW	to save CC
000046C6	E750 5048 080E		00004680	3326+	VST	V21, V1069	save v1 output
000046CC	07FB			3327+	BR	R11	return
000046D0				3328+RE69	DC	0F	V1 for this test
000046D0				3329+	DROP	R5	
000046D0	00000000 00000000			3330	DC	XL16' 0000000000000000 0000000000000000'	result
000046D8	00000000 00000000						
000046E0	FFFFFFFF FFFFFFFF			3331	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000046E8	FFFFFFFF FFFFFFFF						
000046F0	00000000 00000000			3332	DC	XL16' 0000000000000000 0000000000000000'	v3
000046F8	00000000 00000000						
				3333			
				3334 *Hal fword			
				3335	VRR_B	VCEQ, 1, 0	
00004700				3336+	DS	0FD	
00004700		00004700		3337+	USING	*, R5	base for test data and test routine
00004700	00004768			3338+T70	DC	A(X70)	address of test routine
00004704	0046			3339+	DC	H' 70'	test number
00004706	00			3340+	DC	X' 00'	
00004707	01			3341+	DC	HL1' 1'	m4 used
00004708	01			3342+	DC	HL1' 1'	m5 used
00004709	00			3343+	DC	HL1' 0'	CC
0000470A	07			3344+	DC	HL1' 7'	CC failed mask
0000470C	00000000 00000000			3345+	DS	2F	extracted PSW after test (has CC)
00004714	FF			3346+	DC	X' FF'	extracted CC, if test failed
00004715	E5C3C5D8 40404040			3347+	DC	CL8' VCEQ'	instruction name
00004720	00004798			3348+	DC	A(RE70)	address of v1 result
00004724	000047A8			3349+	DC	A(RE70+16)	address of v2 source
00004728	000047B8			3350+	DC	A(RE70+32)	address of v3 source
0000472C	00000010			3351+	DC	A(16)	result length
00004730	00004798			3352+REA70	DC	A(RE70)	result address
00004738	00000000 00000000			3353+	DS	2FD	gap
00004740	00000000 00000000						
00004748	00000000 00000000			3354+V1070	DS	XL16	V1 output
00004750	00000000 00000000						
00004758	00000000 00000000			3355+	DS	2FD	gap
00004760	00000000 00000000						
				3356+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004768				3357+X70	DS	0F	
00004768	E310 5024 0014		00000024	3358+	LGF	R1, V2ADDR	load v2 source
0000476E	E761 0000 0806		00000000	3359+	VL	v22, 0(R1)	use v21 to test decoder
00004774	E310 5028 0014		00000028	3360+	LGF	R1, V3ADDR	load v3 source
0000477A	E771 0000 0806		00000000	3361+	VL	v23, 0(R1)	use v22 to test decoder
00004780	E756 7010 1EF8			3362+	VCEQ	V21, V22, V23, 1, 1	test instruction
00004786	B98D 0020			3363+	EPSW	R2, R0	extract psw
0000478A	5020 500C		0000000C	3364+	ST	R2, CCPSW	to save CC
0000478E	E750 5048 080E		00004748	3365+	VST	V21, V1070	save v1 output
00004794	07FB			3366+	BR	R11	return
00004798				3367+RE70	DC	0F	V1 for this test
00004798				3368+	DROP	R5	
00004798	FFFFFFFF FFFFFFFF			3369	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000047A0	FFFFFFFF FFFFFFFF						
000047A8	00000000 00000000			3370	DC	XL16' 0000000000000000 0000000000000000'	v2
000047B0	00000000 00000000						
000047B8	00000000 00000000			3371	DC	XL16' 0000000000000000 0000000000000000'	v3
000047C0	00000000 00000000						
				3372			
				3373	VRR_B	VCEQ, 1, 1	
000047C8				3374+	DS	0FD	
000047C8		000047C8		3375+	USING	*, R5	base for test data and test routine
000047C8	00004830			3376+T71	DC	A(X71)	address of test routine
000047CC	0047			3377+	DC	H' 71'	test number
000047CE	00			3378+	DC	X' 00'	
000047CF	01			3379+	DC	HL1' 1'	m4 used
000047D0	01			3380+	DC	HL1' 1'	m5 used
000047D1	01			3381+	DC	HL1' 1'	CC
000047D2	0B			3382+	DC	HL1' 11'	CC failed mask
000047D4	00000000 00000000			3383+	DS	2F	extracted PSW after test (has CC)
000047DC	FF			3384+	DC	X' FF'	extracted CC, if test failed
000047DD	E5C3C5D8 40404040			3385+	DC	CL8' VCEQ'	instruction name
000047E8	00004860			3386+	DC	A(RE71)	address of v1 result
000047EC	00004870			3387+	DC	A(RE71+16)	address of v2 source
000047F0	00004880			3388+	DC	A(RE71+32)	address of v3 source
000047F4	00000010			3389+	DC	A(16)	result length
000047F8	00004860			3390+REA71	DC	A(RE71)	result address
00004800	00000000 00000000			3391+	DS	2FD	gap
00004808	00000000 00000000						
00004810	00000000 00000000			3392+V1071	DS	XL16	V1 output
00004818	00000000 00000000						
00004820	00000000 00000000			3393+	DS	2FD	gap
00004828	00000000 00000000						
				3394+*			
00004830				3395+X71	DS	0F	
00004830	E310 5024 0014		00000024	3396+	LGF	R1, V2ADDR	load v2 source
00004836	E761 0000 0806		00000000	3397+	VL	v22, 0(R1)	use v21 to test decoder
0000483C	E310 5028 0014		00000028	3398+	LGF	R1, V3ADDR	load v3 source
00004842	E771 0000 0806		00000000	3399+	VL	v23, 0(R1)	use v22 to test decoder
00004848	E756 7010 1EF8			3400+	VCEQ	V21, V22, V23, 1, 1	test instruction
0000484E	B98D 0020			3401+	EPSW	R2, R0	extract psw
00004852	5020 500C		0000000C	3402+	ST	R2, CCPSW	to save CC
00004856	E750 5048 080E		00004810	3403+	VST	V21, V1071	save v1 output
0000485C	07FB			3404+	BR	R11	return
00004860				3405+RE71	DC	0F	V1 for this test
00004860				3406+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004860	FFFFFFFF FFFFFFFF			3407	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result
00004868	00000000 FFFFFFFF						
00004870	00000000 00000000			3408	DC	XL16' 0000000000000000 0000000000000000'	v2
00004878	00000000 00000000						
00004880	00000000 00000000			3409	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00004888	8FFF8FFF 00000000						
				3410			
				3411	VRR_B	VCEQ, 1, 3	
00004890				3412+	DS	0FD	
00004890		00004890		3413+	USING	*, R5	base for test data and test routine
00004890	000048F8			3414+T72	DC	A(X72)	address of test routine
00004894	0048			3415+	DC	H' 72'	test number
00004896	00			3416+	DC	X' 00'	
00004897	01			3417+	DC	HL1' 1'	m4 used
00004898	01			3418+	DC	HL1' 1'	m5 used
00004899	03			3419+	DC	HL1' 3'	CC
0000489A	0E			3420+	DC	HL1' 14'	CC failed mask
0000489C	00000000 00000000			3421+	DS	2F	extracted PSW after test (has CC)
000048A4	FF			3422+	DC	X' FF'	extracted CC, if test failed
000048A5	E5C3C5D8 40404040			3423+	DC	CL8' VCEQ'	instruction name
000048B0	00004928			3424+	DC	A(RE72)	address of v1 result
000048B4	00004938			3425+	DC	A(RE72+16)	address of v2 source
000048B8	00004948			3426+	DC	A(RE72+32)	address of v3 source
000048BC	00000010			3427+	DC	A(16)	result length
000048C0	00004928			3428+REA72	DC	A(RE72)	result address
000048C8	00000000 00000000			3429+	DS	2FD	gap
000048D0	00000000 00000000						
000048D8	00000000 00000000			3430+V1072	DS	XL16	V1 output
000048E0	00000000 00000000						
000048E8	00000000 00000000			3431+	DS	2FD	gap
000048F0	00000000 00000000						
				3432+*			
000048F8				3433+X72	DS	0F	
000048F8	E310 5024 0014		00000024	3434+	LGF	R1, V2ADDR	load v2 source
000048FE	E761 0000 0806		00000000	3435+	VL	v22, 0(R1)	use v21 to test decoder
00004904	E310 5028 0014		00000028	3436+	LGF	R1, V3ADDR	load v3 source
0000490A	E771 0000 0806		00000000	3437+	VL	v23, 0(R1)	use v22 to test decoder
00004910	E756 7010 1EF8			3438+	VCEQ	V21, V22, V23, 1, 1	test instruction
00004916	B98D 0020			3439+	EPSW	R2, R0	extract psw
0000491A	5020 500C		0000000C	3440+	ST	R2, CCPSW	to save CC
0000491E	E750 5048 080E		000048D8	3441+	VST	V21, V1072	save v1 output
00004924	07FB			3442+	BR	R11	return
00004928				3443+RE72	DC	0F	V1 for this test
00004928				3444+	DROP	R5	
00004928	00000000 00000000			3445	DC	XL16' 0000000000000000 0000000000000000'	result
00004930	00000000 00000000						
00004938	FFFFFFFF FFFFFFFF			3446	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00004940	FFFFFFFF FFFFFFFF						
00004948	00000000 00000000			3447	DC	XL16' 0000000000000000 0000000000000000'	v3
00004950	00000000 00000000						
				3448			
				3449 *Word			
				3450	VRR_B	VCEQ, 2, 0	
00004958				3451+	DS	0FD	
00004958		00004958		3452+	USING	*, R5	base for test data and test routine
00004958	000049C0			3453+T73	DC	A(X73)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000495C	0049			3454+	DC	H' 73'	test number
0000495E	00			3455+	DC	X' 00'	
0000495F	02			3456+	DC	HL1' 2'	m4 used
00004960	01			3457+	DC	HL1' 1'	m5 used
00004961	00			3458+	DC	HL1' 0'	CC
00004962	07			3459+	DC	HL1' 7'	CC failed mask
00004964	00000000 00000000			3460+	DS	2F	extracted PSW after test (has CC)
0000496C	FF			3461+	DC	X' FF'	extracted CC, if test failed
0000496D	E5C3C5D8 40404040			3462+	DC	CL8' VCEQ'	instruction name
00004978	000049F0			3463+	DC	A(RE73)	address of v1 result
0000497C	00004A00			3464+	DC	A(RE73+16)	address of v2 source
00004980	00004A10			3465+	DC	A(RE73+32)	address of v3 source
00004984	00000010			3466+	DC	A(16)	result length
00004988	000049F0			3467+REA73	DC	A(RE73)	result address
00004990	00000000 00000000			3468+	DS	2FD	gap
00004998	00000000 00000000						
000049A0	00000000 00000000			3469+V1073	DS	XL16	V1 output
000049A8	00000000 00000000						
000049B0	00000000 00000000			3470+	DS	2FD	gap
000049B8	00000000 00000000						
000049C0				3471+*			
000049C0	E310 5024 0014			3472+X73	DS	0F	
000049C6	E761 0000 0806		00000024	3473+	LGF	R1, V2ADDR	load v2 source
000049CC	E310 5028 0014		00000000	3474+	VL	v22, 0(R1)	use v21 to test decoder
000049D2	E771 0000 0806		00000028	3475+	LGF	R1, V3ADDR	load v3 source
000049D8	E756 7010 2EF8		00000000	3476+	VL	v23, 0(R1)	use v22 to test decoder
000049DE	B98D 0020			3477+	VCEQ	V21, V22, V23, 2, 1	test instruction
000049E2	B98D 0020			3478+	EPSW	R2, R0	extract psw
000049E2	5020 500C		0000000C	3479+	ST	R2, CCPSW	to save CC
000049E6	E750 5048 080E		000049A0	3480+	VST	V21, V1073	save v1 output
000049EC	07FB			3481+	BR	R11	return
000049F0				3482+RE73	DC	0F	V1 for this test
000049F0				3483+	DROP	R5	
000049F0	FFFFFFFF FFFFFFFF			3484	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000049F8	FFFFFFFF FFFFFFFF						
00004A00	00000000 00000000			3485	DC	XL16' 0000000000000000 0000000000000000'	v2
00004A08	00000000 00000000						
00004A10	00000000 00000000			3486	DC	XL16' 0000000000000000 0000000000000000'	v3
00004A18	00000000 00000000						
00004A20				3487			
00004A20				3488	VRR_B	VCEQ, 2, 1	
00004A20		00004A20		3489+	DS	0FD	
00004A20	00004A88			3490+	USING	*, R5	base for test data and test routine
00004A24	004A			3491+T74	DC	A(X74)	address of test routine
00004A26	00			3492+	DC	H' 74'	test number
00004A27	02			3493+	DC	X' 00'	
00004A28	01			3494+	DC	HL1' 2'	m4 used
00004A29	01			3495+	DC	HL1' 1'	m5 used
00004A2A	0B			3496+	DC	HL1' 1'	CC
00004A2A	0B			3497+	DC	HL1' 11'	CC failed mask
00004A2C	00000000 00000000			3498+	DS	2F	extracted PSW after test (has CC)
00004A34	FF			3499+	DC	X' FF'	extracted CC, if test failed
00004A35	E5C3C5D8 40404040			3500+	DC	CL8' VCEQ'	instruction name
00004A40	00004AB8			3501+	DC	A(RE74)	address of v1 result
00004A44	00004AC8			3502+	DC	A(RE74+16)	address of v2 source
00004A48	00004AD8			3503+	DC	A(RE74+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004A4C	00000010			3504+	DC	A(16)	result length
00004A50	00004AB8			3505+REA74	DC	A(RE74)	result address
00004A58	00000000 00000000			3506+	DS	2FD	gap
00004A60	00000000 00000000						
00004A68	00000000 00000000			3507+V1074	DS	XL16	V1 output
00004A70	00000000 00000000						
00004A78	00000000 00000000			3508+	DS	2FD	gap
00004A80	00000000 00000000						
				3509+*			
00004A88				3510+X74	DS	0F	
00004A88	E310 5024 0014		00000024	3511+	LGF	R1, V2ADDR	load v2 source
00004A8E	E761 0000 0806		00000000	3512+	VL	v22, 0(R1)	use v21 to test decoder
00004A94	E310 5028 0014		00000028	3513+	LGF	R1, V3ADDR	load v3 source
00004A9A	E771 0000 0806		00000000	3514+	VL	v23, 0(R1)	use v22 to test decoder
00004AA0	E756 7010 2EF8			3515+	VCEQ	V21, V22, V23, 2, 1	test instruction
00004AA6	B98D 0020			3516+	EPSW	R2, R0	extract psw
00004AAA	5020 500C		0000000C	3517+	ST	R2, CCPSW	to save CC
00004AAE	E750 5048 080E		00004A68	3518+	VST	V21, V1074	save v1 output
00004AB4	07FB			3519+	BR	R11	return
00004AB8				3520+RE74	DC	0F	V1 for this test
00004AB8				3521+	DROP	R5	
00004AB8	FFFFFFFF FFFFFFFF			3522	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result
00004AC0	00000000 FFFFFFFF						
00004AC8	00000000 00000000			3523	DC	XL16' 0000000000000000 0000000000000000'	v2
00004AD0	00000000 00000000						
00004AD8	00000000 00000000			3524	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00004AE0	8FFF8FFF 00000000						
				3525			
				3526	VRR_B	VCEQ, 2, 3	
00004AE8				3527+	DS	0FD	
00004AE8		00004AE8		3528+	USING	*, R5	base for test data and test routine
00004AE8	00004B50			3529+T75	DC	A(X75)	address of test routine
00004AEC	004B			3530+	DC	H' 75'	test number
00004AEE	00			3531+	DC	X' 00'	
00004AEF	02			3532+	DC	HL1' 2'	m4 used
00004AF0	01			3533+	DC	HL1' 1'	m5 used
00004AF1	03			3534+	DC	HL1' 3'	CC
00004AF2	0E			3535+	DC	HL1' 14'	CC failed mask
00004AF4	00000000 00000000			3536+	DS	2F	extracted PSW after test (has CC)
00004AFC	FF			3537+	DC	X' FF'	extracted CC, if test failed
00004AFD	E5C3C5D8 40404040			3538+	DC	CL8' VCEQ'	instruction name
00004B08	00004B80			3539+	DC	A(RE75)	address of v1 result
00004B0C	00004B90			3540+	DC	A(RE75+16)	address of v2 source
00004B10	00004BA0			3541+	DC	A(RE75+32)	address of v3 source
00004B14	00000010			3542+	DC	A(16)	result length
00004B18	00004B80			3543+REA75	DC	A(RE75)	result address
00004B20	00000000 00000000			3544+	DS	2FD	gap
00004B28	00000000 00000000						
00004B30	00000000 00000000			3545+V1075	DS	XL16	V1 output
00004B38	00000000 00000000						
00004B40	00000000 00000000			3546+	DS	2FD	gap
00004B48	00000000 00000000						
				3547+*			
00004B50				3548+X75	DS	0F	
00004B50	E310 5024 0014		00000024	3549+	LGF	R1, V2ADDR	load v2 source
00004B56	E761 0000 0806		00000000	3550+	VL	v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004B5C	E310 5028 0014		00000028	3551+	LGF	R1, V3ADDR	load v3 source
00004B62	E771 0000 0806		00000000	3552+	VL	v23, 0(R1)	use v22 to test decoder
00004B68	E756 7010 2EF8			3553+	VCEQ	V21, V22, V23, 2, 1	test instruction
00004B6E	B98D 0020			3554+	EPSW	R2, R0	extract psw
00004B72	5020 500C		0000000C	3555+	ST	R2, CCPSW	to save CC
00004B76	E750 5048 080E		00004B30	3556+	VST	V21, V1075	save v1 output
00004B7C	07FB			3557+	BR	R11	return
00004B80				3558+RE75	DC	0F	V1 for this test
00004B80				3559+	DROP	R5	
00004B80	00000000 00000000			3560	DC	XL16' 0000000000000000 0000000000000000'	result t
00004B88	00000000 00000000						
00004B90	FFFFFFFF FFFFFFFF			3561	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00004B98	FFFFFFFF FFFFFFFF						
00004BA0	00000000 00000000			3562	DC	XL16' 0000000000000000 0000000000000000'	v3
00004BA8	00000000 00000000						
				3563			
				3564 *Doubleword			
00004BB0				3565	VRR_B	VCEQ, 3, 0	
00004BB0		00004BB0		3566+	DS	0FD	
00004BB0	00004C18			3567+	USING	*, R5	base for test data and test routine
00004BB4	004C			3568+T76	DC	A(X76)	address of test routine
00004BB6	00			3569+	DC	H' 76'	test number
00004BB7	03			3570+	DC	X' 00'	
00004BB8	01			3571+	DC	HL1' 3'	m4 used
00004BB8	01			3572+	DC	HL1' 1'	m5 used
00004BB9	00			3573+	DC	HL1' 0'	CC
00004BBA	07			3574+	DC	HL1' 7'	CC failed mask
00004BBC	00000000 00000000			3575+	DS	2F	extracted PSW after test (has CC)
00004BC4	FF			3576+	DC	X' FF'	extracted CC, if test failed
00004BC5	E5C3C5D8 40404040			3577+	DC	CL8' VCEQ'	instruction name
00004BD0	00004C48			3578+	DC	A(RE76)	address of v1 result
00004BD4	00004C58			3579+	DC	A(RE76+16)	address of v2 source
00004BD8	00004C68			3580+	DC	A(RE76+32)	address of v3 source
00004BDC	00000010			3581+	DC	A(16)	result length
00004BE0	00004C48			3582+REA76	DC	A(RE76)	result address
00004BE8	00000000 00000000			3583+	DS	2FD	gap
00004BF0	00000000 00000000						
00004BF8	00000000 00000000			3584+V1076	DS	XL16	V1 output
00004C00	00000000 00000000						
00004C08	00000000 00000000			3585+	DS	2FD	gap
00004C10	00000000 00000000						
				3586+*			
00004C18				3587+X76	DS	0F	
00004C18	E310 5024 0014		00000024	3588+	LGF	R1, V2ADDR	load v2 source
00004C1E	E761 0000 0806		00000000	3589+	VL	v22, 0(R1)	use v21 to test decoder
00004C24	E310 5028 0014		00000028	3590+	LGF	R1, V3ADDR	load v3 source
00004C2A	E771 0000 0806		00000000	3591+	VL	v23, 0(R1)	use v22 to test decoder
00004C30	E756 7010 3EF8			3592+	VCEQ	V21, V22, V23, 3, 1	test instruction
00004C36	B98D 0020			3593+	EPSW	R2, R0	extract psw
00004C3A	5020 500C		0000000C	3594+	ST	R2, CCPSW	to save CC
00004C3E	E750 5048 080E		00004BF8	3595+	VST	V21, V1076	save v1 output
00004C44	07FB			3596+	BR	R11	return
00004C48				3597+RE76	DC	0F	V1 for this test
00004C48				3598+	DROP	R5	
00004C48	FFFFFFFF FFFFFFFF			3599	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00004C50	FFFFFFFF FFFFFFFF						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00004C58	00000000 00000000			3600	DC	XL16' 0000000000000000 0000000000000000'	v2	
00004C60	00000000 00000000							
00004C68	00000000 00000000			3601	DC	XL16' 0000000000000000 0000000000000000'	v3	
00004C70	00000000 00000000							
				3602				
				3603	VRR_B	VCEQ, 3, 1		
00004C78				3604+	DS	OFD		
00004C78		00004C78		3605+	USING	*, R5	base for test data and test routine	
00004C78	00004CE0			3606+T77	DC	A(X77)	address of test routine	
00004C7C	004D			3607+	DC	H' 77'	test number	
00004C7E	00			3608+	DC	X' 00'		
00004C7F	03			3609+	DC	HL1' 3'	m4 used	
00004C80	01			3610+	DC	HL1' 1'	m5 used	
00004C81	01			3611+	DC	HL1' 1'	CC	
00004C82	0B			3612+	DC	HL1' 11'	CC failed mask	
00004C84	00000000 00000000			3613+	DS	2F	extracted PSW after test (has CC)	
00004C8C	FF			3614+	DC	X' FF'	extracted CC, if test failed	
00004C8D	E5C3C5D8 40404040			3615+	DC	CL8' VCEQ'	instruction name	
00004C98	00004D10			3616+	DC	A(RE77)	address of v1 result	
00004C9C	00004D20			3617+	DC	A(RE77+16)	address of v2 source	
00004CA0	00004D30			3618+	DC	A(RE77+32)	address of v3 source	
00004CA4	00000010			3619+	DC	A(16)	result length	
00004CA8	00004D10			3620+REA77	DC	A(RE77)	result address	
00004CB0	00000000 00000000			3621+	DS	2FD	gap	
00004CB8	00000000 00000000							
00004CC0	00000000 00000000			3622+V1077	DS	XL16	V1 output	
00004CC8	00000000 00000000							
00004CD0	00000000 00000000			3623+	DS	2FD	gap	
00004CD8	00000000 00000000							
				3624+*				
00004CE0				3625+X77	DS	0F		
00004CE0	E310 5024 0014		00000024	3626+	LGF	R1, V2ADDR	load v2 source	
00004CE6	E761 0000 0806		00000000	3627+	VL	v22, 0(R1)	use v21 to test decoder	
00004CEC	E310 5028 0014		00000028	3628+	LGF	R1, V3ADDR	load v3 source	
00004CF2	E771 0000 0806		00000000	3629+	VL	v23, 0(R1)	use v22 to test decoder	
00004CF8	E756 7010 3EF8			3630+	VCEQ	V21, V22, V23, 3, 1	test instruction	
00004CFE	B98D 0020			3631+	EPSW	R2, R0	extract psw	
00004D02	5020 500C		0000000C	3632+	ST	R2, CCPSW	to save CC	
00004D06	E750 5048 080E		00004CC0	3633+	VST	V21, V1077	save v1 output	
00004D0C	07FB			3634+	BR	R11	return	
00004D10				3635+RE77	DC	0F	V1 for this test	
00004D10				3636+	DROP	R5		
00004D10	FFFFFFFF FFFFFFFF			3637	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result t	
00004D18	00000000 00000000							
00004D20	00000000 00000000			3638	DC	XL16' 0000000000000000 0000000000000000'	v2	
00004D28	00000000 00000000							
00004D30	00000000 00000000			3639	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3	
00004D38	8FFF8FFF 00000000							
				3640				
				3641	VRR_B	VCEQ, 3, 3		
00004D40				3642+	DS	OFD		
00004D40		00004D40		3643+	USING	*, R5	base for test data and test routine	
00004D40	00004DA8			3644+T78	DC	A(X78)	address of test routine	
00004D44	004E			3645+	DC	H' 78'	test number	
00004D46	00			3646+	DC	X' 00'		
00004D47	03			3647+	DC	HL1' 3'	m4 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00004D48	01			3648+	DC	HL1' 1' m5 used
00004D49	03			3649+	DC	HL1' 3' CC
00004D4A	0E			3650+	DC	HL1' 14' CC failed mask
00004D4C	00000000 00000000			3651+	DS	2F extracted PSW after test (has CC)
00004D54	FF			3652+	DC	X' FF' extracted CC, if test failed
00004D55	E5C3C5D8 40404040			3653+	DC	CL8' VCEQ' instruction name
00004D60	00004DD8			3654+	DC	A(RE78) address of v1 result
00004D64	00004DE8			3655+	DC	A(RE78+16) address of v2 source
00004D68	00004DF8			3656+	DC	A(RE78+32) address of v3 source
00004D6C	00000010			3657+	DC	A(16) result length
00004D70	00004DD8			3658+REA78	DC	A(RE78) result address
00004D78	00000000 00000000			3659+	DS	2FD gap
00004D80	00000000 00000000					
00004D88	00000000 00000000			3660+V1078	DS	XL16 V1 output
00004D90	00000000 00000000					
00004D98	00000000 00000000			3661+	DS	2FD gap
00004DA0	00000000 00000000					
00004DA8				3662+*		
00004DA8	E310 5024 0014		00000024	3663+X78	DS	0F
00004DAE	E761 0000 0806		00000000	3664+	LGF	R1, V2ADDR load v2 source
00004DB4	E310 5028 0014		00000028	3665+	VL	v22, 0(R1) use v21 to test decoder
00004DBA	E771 0000 0806		00000000	3666+	LGF	R1, V3ADDR load v3 source
00004DC0	E756 7010 3EF8			3667+	VL	v23, 0(R1) use v22 to test decoder
00004DC6	B98D 0020			3668+	VCEQ	V21, V22, V23, 3, 1 test instruction
00004DCA	5020 500C		0000000C	3669+	EPSW	R2, R0 extract psw
00004DCE	E750 5048 080E		00004D88	3670+	ST	R2, CCPSW to save CC
00004DD4	07FB			3671+	VST	V21, V1078 save v1 output
00004DD8				3672+	BR	R11 return
00004DD8				3673+RE78	DC	0F V1 for this test
00004DD8				3674+	DROP	R5
00004DD8	00000000 00000000			3675	DC	XL16' 0000000000000000 0000000000000000' result t
00004DE0	00000000 00000000					
00004DE8	FFFFFFFF FFFFFFFF			3676	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF' v2
00004DF0	FFFFFFFF FFFFFFFF					
00004DF8	00000000 00000000			3677	DC	XL16' 0000000000000000 0000000000000000' v3
00004E00	00000000 00000000					
				3678		
				3679 *		-----
				3680 * case -		general
				3681 *		-----
				3682 *Byte		
00004E08				3683	VRR_B	VCEQ, 0, 0
00004E08		00004E08		3684+	DS	0FD
00004E08	00004E70			3685+	USING	*, R5 base for test data and test routine
00004E0C	004F			3686+T79	DC	A(X79) address of test routine
00004E0E	00			3687+	DC	H' 79' test number
00004E0F	00			3688+	DC	X' 00'
00004E10	01			3689+	DC	HL1' 0' m4 used
00004E11	00			3690+	DC	HL1' 1' m5 used
00004E12	07			3691+	DC	HL1' 0' CC
00004E14	00000000 00000000			3692+	DC	HL1' 7' CC failed mask
00004E1C	FF			3693+	DS	2F extracted PSW after test (has CC)
00004E1D	E5C3C5D8 40404040			3694+	DC	X' FF' extracted CC, if test failed
00004E28	00004EA0			3695+	DC	CL8' VCEQ' instruction name
00004E2C	00004EB0			3696+	DC	A(RE79) address of v1 result
				3697+	DC	A(RE79+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004E30	00004EC0			3698+	DC	A(RE79+32)	address of v3 source
00004E34	00000010			3699+	DC	A(16)	result length
00004E38	00004EA0			3700+REA79	DC	A(RE79)	result address
00004E40	00000000 00000000			3701+	DS	2FD	gap
00004E48	00000000 00000000						
00004E50	00000000 00000000			3702+V1079	DS	XL16	V1 output
00004E58	00000000 00000000						
00004E60	00000000 00000000			3703+	DS	2FD	gap
00004E68	00000000 00000000						
00004E70				3704+*			
00004E70	E310 5024 0014		00000024	3705+X79	DS	0F	
00004E76	E761 0000 0806		00000000	3706+	LGF	R1, V2ADDR	load v2 source
00004E7C	E310 5028 0014		00000028	3707+	VL	v22, 0(R1)	use v21 to test decoder
00004E82	E771 0000 0806		00000000	3708+	LGF	R1, V3ADDR	load v3 source
00004E88	E756 7010 0EF8			3709+	VL	v23, 0(R1)	use v22 to test decoder
00004E8E	B98D 0020			3710+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004E92	5020 500C		0000000C	3711+	EPSW	R2, R0	extract psw
00004E96	E750 5048 080E		00004E50	3712+	ST	R2, CCPSW	to save CC
00004E9C	07FB			3713+	VST	V21, V1079	save v1 output
00004EA0				3714+	BR	R11	return
00004EA0				3715+RE79	DC	0F	V1 for this test
00004EA0	FFFFFFFF FFFFFFFF			3716+	DROP	R5	
00004EA8	FFFFFFFF FFFFFFFF			3717	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00004EB0	00110033 00550077			3718	DC	XL16' 0011003300550077 0022004400660008'	v2
00004EB8	00220044 00660008						
00004EC0	00110033 00550077			3719	DC	XL16' 0011003300550077 0022004400660008'	v3
00004EC8	00220044 00660008						
00004ED0				3720			
00004ED0		00004ED0		3721	VRR_B	VCEQ, 0, 0	
00004ED0	00004F38			3722+	DS	0FD	
00004ED4	0050			3723+	USING	*, R5	base for test data and test routine
00004ED6	00			3724+T80	DC	A(X80)	address of test routine
00004ED7	00			3725+	DC	H' 80'	test number
00004ED8	01			3726+	DC	X' 00'	
00004ED9	00			3727+	DC	HL1' 0'	m4 used
00004EDA	07			3728+	DC	HL1' 1'	m5 used
00004EDC	00000000 00000000			3729+	DC	HL1' 0'	CC
00004EE4	FF			3730+	DC	HL1' 7'	CC failed mask
00004EE5	E5C3C5D8 40404040			3731+	DS	2F	extracted PSW after test (has CC)
00004EF0	00004F68			3732+	DC	X' FF'	extracted CC, if test failed
00004EF4	00004F78			3733+	DC	CL8' VCEQ'	instruction name
00004EF8	00004F88			3734+	DC	A(RE80)	address of v1 result
00004EFC	00000010			3735+	DC	A(RE80+16)	address of v2 source
00004F00	00004F68			3736+	DC	A(RE80+32)	address of v3 source
00004F08	00000000 00000000			3737+	DC	A(16)	result length
00004F10	00000000 00000000			3738+REA80	DC	A(RE80)	result address
00004F18	00000000 00000000			3739+	DS	2FD	gap
00004F20	00000000 00000000			3740+V1080	DS	XL16	V1 output
00004F28	00000000 00000000						
00004F30	00000000 00000000			3741+	DS	2FD	gap
00004F38				3742+*			
00004F38	E310 5024 0014		00000024	3743+X80	DS	0F	
				3744+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004F3E	E761 0000 0806		00000000	3745+	VL	v22, 0(R1)	use v21 to test decoder
00004F44	E310 5028 0014		00000028	3746+	LGF	R1, V3ADDR	load v3 source
00004F4A	E771 0000 0806		00000000	3747+	VL	v23, 0(R1)	use v22 to test decoder
00004F50	E756 7010 0EF8			3748+	VCEQ	V21, V22, V23, 0, 1	test instruction
00004F56	B98D 0020			3749+	EPSW	R2, R0	extract psw
00004F5A	5020 500C		0000000C	3750+	ST	R2, CCPSW	to save CC
00004F5E	E750 5048 080E		00004F18	3751+	VST	V21, V1080	save v1 output
00004F64	07FB			3752+	BR	R11	return
00004F68				3753+RE80	DC	0F	V1 for this test
00004F68				3754+	DROP	R5	
00004F68	FFFFFFFF FFFFFFFF			3755	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00004F70	FFFFFFFF FFFFFFFF						
00004F78	FFFEFFFD FFFCFFFB			3756	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00004F80	FFFAFFF9 FFF8FFF7						
00004F88	FFFEFFFD FFFCFFFB			3757	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00004F90	FFFAFFF9 FFF8FFF7						
				3758			
00004F98				3759	VRR_B	VCEQ, 0, 1	
00004F98		00004F98		3760+	DS	0FD	
00004F98	00005000			3761+	USING	*, R5	base for test data and test routine
00004F9C	0051			3762+T81	DC	A(X81)	address of test routine
00004F9E	00			3763+	DC	H' 81'	test number
00004F9E	00			3764+	DC	X' 00'	
00004F9F	00			3765+	DC	HL1' 0'	m4 used
00004FA0	01			3766+	DC	HL1' 1'	m5 used
00004FA1	01			3767+	DC	HL1' 1'	CC
00004FA2	0B			3768+	DC	HL1' 11'	CC failed mask
00004FA4	00000000 00000000			3769+	DS	2F	extracted PSW after test (has CC)
00004FAC	FF			3770+	DC	X' FF'	extracted CC, if test failed
00004FAD	E5C3C5D8 40404040			3771+	DC	CL8' VCEQ'	instruction name
00004FB8	00005030			3772+	DC	A(RE81)	address of v1 result
00004FBC	00005040			3773+	DC	A(RE81+16)	address of v2 source
00004FC0	00005050			3774+	DC	A(RE81+32)	address of v3 source
00004FC4	00000010			3775+	DC	A(16)	result length
00004FC8	00005030			3776+REA81	DC	A(RE81)	result address
00004FD0	00000000 00000000			3777+	DS	2FD	gap
00004FD8	00000000 00000000						
00004FE0	00000000 00000000			3778+V1081	DS	XL16	V1 output
00004FE8	00000000 00000000						
00004FF0	00000000 00000000			3779+	DS	2FD	gap
00004FF8	00000000 00000000						
				3780+*			
00005000				3781+X81	DS	0F	
00005000	E310 5024 0014		00000024	3782+	LGF	R1, V2ADDR	load v2 source
00005006	E761 0000 0806		00000000	3783+	VL	v22, 0(R1)	use v21 to test decoder
0000500C	E310 5028 0014		00000028	3784+	LGF	R1, V3ADDR	load v3 source
00005012	E771 0000 0806		00000000	3785+	VL	v23, 0(R1)	use v22 to test decoder
00005018	E756 7010 0EF8			3786+	VCEQ	V21, V22, V23, 0, 1	test instruction
0000501E	B98D 0020			3787+	EPSW	R2, R0	extract psw
00005022	5020 500C		0000000C	3788+	ST	R2, CCPSW	to save CC
00005026	E750 5048 080E		00004FE0	3789+	VST	V21, V1081	save v1 output
0000502C	07FB			3790+	BR	R11	return
00005030				3791+RE81	DC	0F	V1 for this test
00005030				3792+	DROP	R5	
00005030	FF000000 00000000			3793	DC	XL16' FF00000000000000 FFFFFFFFFFFFFFFFFF'	result t
00005038	FFFFFFFF FFFFFFFF						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00005040	00010203 04050607			3794	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2	
00005048	08090A0B 0C0DFE0F							
00005050	00110033 00550077			3795	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v3	
00005058	08090A0B 0C0DFE0F							
				3796				
00005060				3797	VRR_B	VCEQ, 0, 1		
00005060		00005060		3798+	DS	0FD		
00005060	000050C8			3799+	USING	*, R5	base for test data and test routine	
00005064	0052			3800+T82	DC	A(X82)	address of test routine	
00005066	00			3801+	DC	H' 82'	test number	
00005067	00			3802+	DC	X' 00'		
00005068	01			3803+	DC	HL1' 0'	m4 used	
00005068	01			3804+	DC	HL1' 1'	m5 used	
00005069	01			3805+	DC	HL1' 1'	CC	
0000506A	0B			3806+	DC	HL1' 11'	CC failed mask	
0000506C	00000000 00000000			3807+	DS	2F	extracted PSW after test (has CC)	
00005074	FF			3808+	DC	X' FF'	extracted CC, if test failed	
00005075	E5C3C5D8 40404040			3809+	DC	CL8' VCEQ'	instruction name	
00005080	000050F8			3810+	DC	A(RE82)	address of v1 result	
00005084	00005108			3811+	DC	A(RE82+16)	address of v2 source	
00005088	00005118			3812+	DC	A(RE82+32)	address of v3 source	
0000508C	00000010			3813+	DC	A(16)	result length	
00005090	000050F8			3814+REA82	DC	A(RE82)	result address	
00005098	00000000 00000000			3815+	DS	2FD	gap	
000050A0	00000000 00000000							
000050A8	00000000 00000000			3816+V1082	DS	XL16	V1 output	
000050B0	00000000 00000000							
000050B8	00000000 00000000			3817+	DS	2FD	gap	
000050C0	00000000 00000000							
				3818+*				
000050C8				3819+X82	DS	0F		
000050C8	E310 5024 0014		00000024	3820+	LGF	R1, V2ADDR	load v2 source	
000050CE	E761 0000 0806		00000000	3821+	VL	v22, 0(R1)	use v21 to test decoder	
000050D4	E310 5028 0014		00000028	3822+	LGF	R1, V3ADDR	load v3 source	
000050DA	E771 0000 0806		00000000	3823+	VL	v23, 0(R1)	use v22 to test decoder	
000050E0	E756 7010 0EF8			3824+	VCEQ	V21, V22, V23, 0, 1	test instruction	
000050E6	B98D 0020			3825+	EPSW	R2, R0	extract psw	
000050EA	5020 500C		0000000C	3826+	ST	R2, CCPSW	to save CC	
000050EE	E750 5048 080E		000050A8	3827+	VST	V21, V1082	save v1 output	
000050F4	07FB			3828+	BR	R11	return	
000050F8				3829+RE82	DC	0F	V1 for this test	
000050F8				3830+	DROP	R5		
000050F8	FFFFFFFF FFFFFFFF			3831	DC	XL16' FFFFFFFFFFFFFFFFFF FF00000000000000'	result t	
00005100	FF000000 00000000							
00005108	08090A0B 0C0DFE0F			3832	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2	
00005110	00010203 04050607							
00005118	08090A0B 0C0DFE0F			3833	DC	XL16' 08090A0B0C0DFE0F 0011003300550077'	v3	
00005120	00110033 00550077							
				3834				
00005128				3835	VRR_B	VCEQ, 0, 3		
00005128		00005128		3836+	DS	0FD		
00005128	00005190			3837+	USING	*, R5	base for test data and test routine	
0000512C	0053			3838+T83	DC	A(X83)	address of test routine	
0000512E	00			3839+	DC	H' 83'	test number	
0000512F	00			3840+	DC	X' 00'		
				3841+	DC	HL1' 0'	m4 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00005130	01			3842+	DC	HL1' 1' m5 used
00005131	03			3843+	DC	HL1' 3' CC
00005132	0E			3844+	DC	HL1' 14' CC failed mask
00005134	00000000 00000000			3845+	DS	2F extracted PSW after test (has CC)
0000513C	FF			3846+	DC	X' FF' extracted CC, if test failed
0000513D	E5C3C5D8 40404040			3847+	DC	CL8' VCEQ' instruction name
00005148	000051C0			3848+	DC	A(RE83) address of v1 result
0000514C	000051D0			3849+	DC	A(RE83+16) address of v2 source
00005150	000051E0			3850+	DC	A(RE83+32) address of v3 source
00005154	00000010			3851+	DC	A(16) result length
00005158	000051C0			3852+REA83	DC	A(RE83) result address
00005160	00000000 00000000			3853+	DS	2FD gap
00005168	00000000 00000000					
00005170	00000000 00000000			3854+V1083	DS	XL16 V1 output
00005178	00000000 00000000					
00005180	00000000 00000000			3855+	DS	2FD gap
00005188	00000000 00000000					
00005190				3856+*		
00005190	E310 5024 0014		00000024	3857+X83	DS	0F
00005196	E761 0000 0806		00000000	3858+	LGF	R1, V2ADDR load v2 source
0000519C	E310 5028 0014		00000028	3859+	VL	v22, 0(R1) use v21 to test decoder
000051A2	E771 0000 0806		00000000	3860+	LGF	R1, V3ADDR load v3 source
000051A8	E756 7010 0EF8			3861+	VL	v23, 0(R1) use v22 to test decoder
000051AE	B98D 0020			3862+	VCEQ	V21, V22, V23, 0, 1 test instruction
000051B2	5020 500C		0000000C	3863+	EPSW	R2, R0 extract psw
000051B6	E750 5048 080E		00005170	3864+	ST	R2, CCPSW to save CC
000051BC	07FB			3865+	VST	V21, V1083 save v1 output
000051C0				3866+	BR	R11 return
000051C0				3867+RE83	DC	0F V1 for this test
000051C0				3868+	DROP	R5
000051C0	00000000 00000000			3869	DC	XL16' 0000000000000000 0000000000000000' result t
000051C8	00000000 00000000					
000051D0	01110133 01550177			3870	DC	XL16' 0111013301550177 019901BB01DD01FF' v2
000051D8	019901BB 01DD01FF					
000051E0	00010203 04050607			3871	DC	XL16' 0001020304050607 08090A0B0C0D0E0F' v3
000051E8	08090A0B 0C0D0E0F					
000051F0				3872		
000051F0				3873	VRR_B	VCEQ, 0, 3
000051F0		000051F0		3874+	DS	0FD
000051F0	00005258			3875+	USING	*, R5 base for test data and test routine
000051F4	0054			3876+T84	DC	A(X84) address of test routine
000051F6	00			3877+	DC	H' 84' test number
000051F7	00			3878+	DC	X' 00'
000051F8	01			3879+	DC	HL1' 0' m4 used
000051F9	03			3880+	DC	HL1' 1' m5 used
000051FA	0E			3881+	DC	HL1' 3' CC
000051FC	00000000 00000000			3882+	DC	HL1' 14' CC failed mask
00005204	FF			3883+	DS	2F extracted PSW after test (has CC)
00005205	E5C3C5D8 40404040			3884+	DC	X' FF' extracted CC, if test failed
00005210	00005288			3885+	DC	CL8' VCEQ' instruction name
00005214	00005298			3886+	DC	A(RE84) address of v1 result
00005218	000052A8			3887+	DC	A(RE84+16) address of v2 source
0000521C	00000010			3888+	DC	A(RE84+32) address of v3 source
00005220	00005288			3889+	DC	A(16) result length
00005228	00000000 00000000			3890+REA84	DC	A(RE84) result address
				3891+	DS	2FD gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005230	00000000 00000000						
00005238	00000000 00000000			3892+V1084	DS	XL16	V1 output
00005240	00000000 00000000						
00005248	00000000 00000000			3893+	DS	2FD	gap
00005250	00000000 00000000						
00005258				3894+*			
00005258	E310 5024 0014		00000024	3895+X84	DS	0F	
0000525E	E761 0000 0806		00000000	3896+	LGF	R1, V2ADDR	load v2 source
00005264	E310 5028 0014		00000028	3897+	VL	v22, 0(R1)	use v21 to test decoder
0000526A	E771 0000 0806		00000000	3898+	LGF	R1, V3ADDR	load v3 source
00005270	E756 7010 0EF8			3899+	VL	v23, 0(R1)	use v22 to test decoder
00005276	B98D 0020			3900+	VCEQ	V21, V22, V23, 0, 1	test instruction
0000527A	5020 500C		0000000C	3901+	EPSW	R2, R0	extract psw
0000527E	E750 5048 080E		00005238	3902+	ST	R2, CCPSW	to save CC
00005284	07FB			3903+	VST	V21, V1084	save v1 output
00005288				3904+	BR	R11	return
00005288				3905+RE84	DC	0F	V1 for this test
00005288				3906+	DROP	R5	
00005288	00000000 00000000			3907	DC	XL16' 0000000000000000 0000000000000000'	result
00005290	00000000 00000000						
00005298	00010203 04050607			3908	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000052A0	08090A0B 0C0D0E0F						
000052A8	01110133 01550177			3909	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
000052B0	019901BB 01DD01FF						
				3910			
				3911 *Hal fword			
				3912	VRR_B	VCEQ, 1, 0	
000052B8				3913+	DS	0FD	
000052B8		000052B8		3914+	USING	*, R5	base for test data and test routine
000052B8	00005320			3915+T85	DC	A(X85)	address of test routine
000052BC	0055			3916+	DC	H' 85'	test number
000052BE	00			3917+	DC	X' 00'	
000052BF	01			3918+	DC	HL1' 1'	m4 used
000052C0	01			3919+	DC	HL1' 1'	m5 used
000052C1	00			3920+	DC	HL1' 0'	CC
000052C2	07			3921+	DC	HL1' 7'	CC failed mask
000052C4	00000000 00000000			3922+	DS	2F	extracted PSW after test (has CC)
000052CC	FF			3923+	DC	X' FF'	extracted CC, if test failed
000052CD	E5C3C5D8 40404040			3924+	DC	CL8' VCEQ'	instruction name
000052D8	00005350			3925+	DC	A(RE85)	address of v1 result
000052DC	00005360			3926+	DC	A(RE85+16)	address of v2 source
000052E0	00005370			3927+	DC	A(RE85+32)	address of v3 source
000052E4	00000010			3928+	DC	A(16)	result length
000052E8	00005350			3929+REA85	DC	A(RE85)	result address
000052F0	00000000 00000000			3930+	DS	2FD	gap
000052F8	00000000 00000000						
00005300	00000000 00000000			3931+V1085	DS	XL16	V1 output
00005308	00000000 00000000						
00005310	00000000 00000000			3932+	DS	2FD	gap
00005318	00000000 00000000						
				3933+*			
00005320				3934+X85	DS	0F	
00005320	E310 5024 0014		00000024	3935+	LGF	R1, V2ADDR	load v2 source
00005326	E761 0000 0806		00000000	3936+	VL	v22, 0(R1)	use v21 to test decoder
0000532C	E310 5028 0014		00000028	3937+	LGF	R1, V3ADDR	load v3 source
00005332	E771 0000 0806		00000000	3938+	VL	v23, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005338	E756 7010 1EF8			3939+	VCEQ	V21, V22, V23, 1, 1	test instruction
0000533E	B98D 0020			3940+	EPSW	R2, R0	extract psw
00005342	5020 500C		0000000C	3941+	ST	R2, CCPSW	to save CC
00005346	E750 5048 080E		00005300	3942+	VST	V21, V1085	save v1 output
0000534C	07FB			3943+	BR	R11	return
00005350				3944+RE85	DC	0F	V1 for this test
00005350				3945+	DROP	R5	
00005350	FFFFFFFF FFFFFFFF			3946	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005358	FFFFFFFF FFFFFFFF						
00005360	00110033 00550077			3947	DC	XL16' 0011003300550077 0022004400660008'	v2
00005368	00220044 00660008						
00005370	00110033 00550077			3948	DC	XL16' 0011003300550077 0022004400660008'	v3
00005378	00220044 00660008						
00005380				3949			
00005380				3950	VRR_B	VCEQ, 1, 0	
00005380		00005380		3951+	DS	0FD	
00005380	000053E8			3952+	USING	*, R5	base for test data and test routine
00005384	0056			3953+T86	DC	A(X86)	address of test routine
00005386	00			3954+	DC	H' 86'	test number
00005387	01			3955+	DC	X' 00'	
00005388	01			3956+	DC	HL1' 1'	m4 used
00005388	01			3957+	DC	HL1' 1'	m5 used
00005389	00			3958+	DC	HL1' 0'	CC
0000538A	07			3959+	DC	HL1' 7'	CC failed mask
0000538C	00000000 00000000			3960+	DS	2F	extracted PSW after test (has CC)
00005394	FF			3961+	DC	X' FF'	extracted CC, if test failed
00005395	E5C3C5D8 40404040			3962+	DC	CL8' VCEQ'	instruction name
000053A0	00005418			3963+	DC	A(RE86)	address of v1 result
000053A4	00005428			3964+	DC	A(RE86+16)	address of v2 source
000053A8	00005438			3965+	DC	A(RE86+32)	address of v3 source
000053AC	00000010			3966+	DC	A(16)	result length
000053B0	00005418			3967+REA86	DC	A(RE86)	result address
000053B8	00000000 00000000			3968+	DS	2FD	gap
000053C0	00000000 00000000						
000053C8	00000000 00000000			3969+V1086	DS	XL16	V1 output
000053D0	00000000 00000000						
000053D8	00000000 00000000			3970+	DS	2FD	gap
000053E0	00000000 00000000						
000053E8				3971+*			
000053E8	E310 5024 0014			3972+X86	DS	0F	
000053EE	E761 0000 0806		00000024	3973+	LGF	R1, V2ADDR	load v2 source
000053F4	E310 5028 0014		00000000	3974+	VL	v22, 0(R1)	use v21 to test decoder
000053FA	E771 0000 0806		00000028	3975+	LGF	R1, V3ADDR	load v3 source
00005400	E756 7010 1EF8		00000000	3976+	VL	v23, 0(R1)	use v22 to test decoder
00005406	B98D 0020			3977+	VCEQ	V21, V22, V23, 1, 1	test instruction
0000540A	5020 500C			3978+	EPSW	R2, R0	extract psw
0000540E	E750 5048 080E		0000000C	3979+	ST	R2, CCPSW	to save CC
00005414	07FB		000053C8	3980+	VST	V21, V1086	save v1 output
00005418				3981+	BR	R11	return
00005418				3982+RE86	DC	0F	V1 for this test
00005418				3983+	DROP	R5	
00005418	FFFFFFFF FFFFFFFF			3984	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005420	FFFFFFFF FFFFFFFF						
00005428	FFFEFFFD FFFCFFFB			3985	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00005430	FFFAFFF9 FFF8FFF7						
00005438	FFFEFFFD FFFCFFFB			3986	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005440	FFFAFFF9 FFF8FFF7			3987			
				3988	VRR_B VCEQ, 1, 1		
00005448				3989+	DS OFD		
00005448		00005448		3990+	USING *, R5	base for test data and test routine	
00005448	000054B0			3991+T87	DC A(X87)	address of test routine	
0000544C	0057			3992+	DC H' 87'	test number	
0000544E	00			3993+	DC X' 00'		
0000544F	01			3994+	DC HL1' 1'	m4 used	
00005450	01			3995+	DC HL1' 1'	m5 used	
00005451	01			3996+	DC HL1' 1'	CC	
00005452	0B			3997+	DC HL1' 11'	CC failed mask	
00005454	00000000 00000000			3998+	DS 2F	extracted PSW after test (has CC)	
0000545C	FF			3999+	DC X' FF'	extracted CC, if test failed	
0000545D	E5C3C5D8 40404040			4000+	DC CL8' VCEQ'	instruction name	
00005468	000054E0			4001+	DC A(RE87)	address of v1 result	
0000546C	000054F0			4002+	DC A(RE87+16)	address of v2 source	
00005470	00005500			4003+	DC A(RE87+32)	address of v3 source	
00005474	00000010			4004+	DC A(16)	result length	
00005478	000054E0			4005+REA87	DC A(RE87)	result address	
00005480	00000000 00000000			4006+	DS 2FD	gap	
00005488	00000000 00000000						
00005490	00000000 00000000			4007+V1087	DS XL16	V1 output	
00005498	00000000 00000000						
000054A0	00000000 00000000			4008+	DS 2FD	gap	
000054A8	00000000 00000000						
				4009+*			
000054B0				4010+X87	DS OF		
000054B0	E310 5024 0014		00000024	4011+	LGF R1, V2ADDR	load v2 source	
000054B6	E761 0000 0806		00000000	4012+	VL v22, 0(R1)	use v21 to test decoder	
000054BC	E310 5028 0014		00000028	4013+	LGF R1, V3ADDR	load v3 source	
000054C2	E771 0000 0806		00000000	4014+	VL v23, 0(R1)	use v22 to test decoder	
000054C8	E756 7010 1EF8			4015+	VCEQ V21, V22, V23, 1, 1	test instruction	
000054CE	B98D 0020			4016+	EPSW R2, R0	extract psw	
000054D2	5020 500C		0000000C	4017+	ST R2, CCPSW	to save CC	
000054D6	E750 5048 080E		00005490	4018+	VST V21, V1087	save v1 output	
000054DC	07FB			4019+	BR R11	return	
000054E0				4020+RE87	DC OF	V1 for this test	
000054E0				4021+	DROP R5		
000054E0	FFFF0000 00000000			4022	DC XL16' FFFF000000000000 FFFFFFFFFFFFFFFF'	result t	
000054E8	FFFFFFFF FFFFFFFF						
000054F0	00010203 04050607			4023	DC XL16' 0001020304050607 08090A0B0C0DFE0F'	v2	
000054F8	08090A0B 0C0DFE0F						
00005500	00010033 00550077			4024	DC XL16' 0001003300550077 08090A0B0C0DFE0F'	v3	
00005508	08090A0B 0C0DFE0F						
				4025			
				4026	VRR_B VCEQ, 1, 1		
00005510				4027+	DS OFD		
00005510		00005510		4028+	USING *, R5	base for test data and test routine	
00005510	00005578			4029+T88	DC A(X88)	address of test routine	
00005514	0058			4030+	DC H' 88'	test number	
00005516	00			4031+	DC X' 00'		
00005517	01			4032+	DC HL1' 1'	m4 used	
00005518	01			4033+	DC HL1' 1'	m5 used	
00005519	01			4034+	DC HL1' 1'	CC	
0000551A	0B			4035+	DC HL1' 11'	CC failed mask	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000551C	00000000 00000000			4036+	DS	2F	extracted PSW after test (has CC)
00005524	FF			4037+	DC	X' FF'	extracted CC, if test failed
00005525	E5C3C5D8 40404040			4038+	DC	CL8' VCEQ'	instruction name
00005530	000055A8			4039+	DC	A(RE88)	address of v1 result
00005534	000055B8			4040+	DC	A(RE88+16)	address of v2 source
00005538	000055C8			4041+	DC	A(RE88+32)	address of v3 source
0000553C	00000010			4042+	DC	A(16)	result length
00005540	000055A8			4043+REA88	DC	A(RE88)	result address
00005548	00000000 00000000			4044+	DS	2FD	gap
00005550	00000000 00000000						
00005558	00000000 00000000			4045+V1088	DS	XL16	V1 output
00005560	00000000 00000000						
00005568	00000000 00000000			4046+	DS	2FD	gap
00005570	00000000 00000000						
				4047+*			
00005578				4048+X88	DS	0F	
00005578	E310 5024 0014		00000024	4049+	LGF	R1, V2ADDR	load v2 source
0000557E	E761 0000 0806		00000000	4050+	VL	v22, 0(R1)	use v21 to test decoder
00005584	E310 5028 0014		00000028	4051+	LGF	R1, V3ADDR	load v3 source
0000558A	E771 0000 0806		00000000	4052+	VL	v23, 0(R1)	use v22 to test decoder
00005590	E756 7010 1EF8			4053+	VCEQ	V21, V22, V23, 1, 1	test instruction
00005596	B98D 0020			4054+	EPSW	R2, R0	extract psw
0000559A	5020 500C		0000000C	4055+	ST	R2, CCPSW	to save CC
0000559E	E750 5048 080E		00005558	4056+	VST	V21, V1088	save v1 output
000055A4	07FB			4057+	BR	R11	return
000055A8				4058+RE88	DC	0F	V1 for this test
000055A8				4059+	DROP	R5	
000055A8	FFFFFFFF FFFFFFFF			4060	DC	XL16' FFFFFFFFFFFFFFFFFF 000000000000FFFF'	result t
000055B0	00000000 0000FFFF						
000055B8	08090A0B 0C0DFE0F			4061	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2
000055C0	00010203 04050607						
000055C8	08090A0B 0C0DFE0F			4062	DC	XL16' 08090A0B0C0DFE0F 0011003300550607'	v3
000055D0	00110033 00550607						
				4063			
				4064	VRR_B	VCEQ, 1, 3	
000055D8				4065+	DS	0FD	
000055D8		000055D8		4066+	USING	*, R5	base for test data and test routine
000055D8	00005640			4067+T89	DC	A(X89)	address of test routine
000055DC	0059			4068+	DC	H' 89'	test number
000055DE	00			4069+	DC	X' 00'	
000055DF	01			4070+	DC	HL1' 1'	m4 used
000055E0	01			4071+	DC	HL1' 1'	m5 used
000055E1	03			4072+	DC	HL1' 3'	CC
000055E2	0E			4073+	DC	HL1' 14'	CC failed mask
000055E4	00000000 00000000			4074+	DS	2F	extracted PSW after test (has CC)
000055EC	FF			4075+	DC	X' FF'	extracted CC, if test failed
000055ED	E5C3C5D8 40404040			4076+	DC	CL8' VCEQ'	instruction name
000055F8	00005670			4077+	DC	A(RE89)	address of v1 result
000055FC	00005680			4078+	DC	A(RE89+16)	address of v2 source
00005600	00005690			4079+	DC	A(RE89+32)	address of v3 source
00005604	00000010			4080+	DC	A(16)	result length
00005608	00005670			4081+REA89	DC	A(RE89)	result address
00005610	00000000 00000000			4082+	DS	2FD	gap
00005618	00000000 00000000						
00005620	00000000 00000000			4083+V1089	DS	XL16	V1 output
00005628	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005630	00000000 00000000			4084+	DS	2FD	gap
00005638	00000000 00000000						
00005640				4085+*			
00005640	E310 5024 0014		00000024	4086+X89	DS	0F	
00005646	E761 0000 0806		00000000	4087+	LGF	R1, V2ADDR	load v2 source
0000564C	E310 5028 0014		00000028	4088+	VL	v22, 0(R1)	use v21 to test decoder
00005652	E771 0000 0806		00000000	4089+	LGF	R1, V3ADDR	load v3 source
00005658	E756 7010 1EF8			4090+	VL	v23, 0(R1)	use v22 to test decoder
0000565E	B98D 0020			4091+	VCEQ	V21, V22, V23, 1, 1	test instruction
00005662	5020 500C		0000000C	4092+	EPSW	R2, R0	extract psw
00005666	E750 5048 080E		00005620	4093+	ST	R2, CCPSW	to save CC
0000566C	07FB			4094+	VST	V21, V1089	save v1 output
00005670				4095+	BR	R11	return
00005670				4096+RE89	DC	0F	V1 for this test
00005670				4097+	DROP	R5	
00005670	00000000 00000000			4098	DC	XL16' 0000000000000000 0000000000000000'	result t
00005678	00000000 00000000						
00005680	01110133 01550177			4099	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00005688	019901BB 01DD01FF						
00005690	00010203 04050607			4100	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00005698	08090A0B 0C0D0E0F						
000056A0				4101			
000056A0				4102	VRR_B	VCEQ, 1, 3	
000056A0		000056A0		4103+	DS	0FD	
000056A0	00005708			4104+	USING	*, R5	base for test data and test routine
000056A4	005A			4105+T90	DC	A(X90)	address of test routine
000056A6	00			4106+	DC	H' 90'	test number
000056A7	01			4107+	DC	X' 00'	
000056A8	01			4108+	DC	HL1' 1'	m4 used
000056A8	01			4109+	DC	HL1' 1'	m5 used
000056A9	03			4110+	DC	HL1' 3'	CC
000056AA	0E			4111+	DC	HL1' 14'	CC failed mask
000056AC	00000000 00000000			4112+	DS	2F	extracted PSW after test (has CC)
000056B4	FF			4113+	DC	X' FF'	extracted CC, if test failed
000056B5	E5C3C5D8 40404040			4114+	DC	CL8' VCEQ'	instruction name
000056C0	00005738			4115+	DC	A(RE90)	address of v1 result
000056C4	00005748			4116+	DC	A(RE90+16)	address of v2 source
000056C8	00005758			4117+	DC	A(RE90+32)	address of v3 source
000056CC	00000010			4118+	DC	A(16)	result length
000056D0	00005738			4119+REA90	DC	A(RE90)	result address
000056D8	00000000 00000000			4120+	DS	2FD	gap
000056E0	00000000 00000000						
000056E8	00000000 00000000			4121+V1090	DS	XL16	V1 output
000056F0	00000000 00000000						
000056F8	00000000 00000000			4122+	DS	2FD	gap
00005700	00000000 00000000						
00005708				4123+*			
00005708	E310 5024 0014		00000024	4124+X90	DS	0F	
0000570E	E761 0000 0806		00000000	4125+	LGF	R1, V2ADDR	load v2 source
00005714	E310 5028 0014		00000028	4126+	VL	v22, 0(R1)	use v21 to test decoder
0000571A	E771 0000 0806		00000000	4127+	LGF	R1, V3ADDR	load v3 source
00005720	E756 7010 1EF8			4128+	VL	v23, 0(R1)	use v22 to test decoder
00005726	B98D 0020			4129+	VCEQ	V21, V22, V23, 1, 1	test instruction
00005726	B98D 0020			4130+	EPSW	R2, R0	extract psw
0000572A	5020 500C		0000000C	4131+	ST	R2, CCPSW	to save CC
0000572E	E750 5048 080E		000056E8	4132+	VST	V21, V1090	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005734	07FB			4133+	BR	R11	return
00005738				4134+RE90	DC	0F	V1 for this test
00005738				4135+	DROP	R5	
00005738	00000000	00000000		4136	DC	XL16' 0000000000000000 0000000000000000'	result t
00005740	00000000	00000000					
00005748	00010203	04050607		4137	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00005750	08090A0B	0C0D0E0F					
00005758	01110133	01550177		4138	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00005760	019901BB	01DD01FF					
				4139			
				4140 *Word			
				4141	VRR_B	VCEQ, 2, 0	
00005768				4142+	DS	0FD	
00005768		00005768		4143+	USING	*, R5	base for test data and test routine
00005768	000057D0			4144+T91	DC	A(X91)	address of test routine
0000576C	005B			4145+	DC	H' 91'	test number
0000576E	00			4146+	DC	X' 00'	
0000576F	02			4147+	DC	HL1' 2'	m4 used
00005770	01			4148+	DC	HL1' 1'	m5 used
00005771	00			4149+	DC	HL1' 0'	CC
00005772	07			4150+	DC	HL1' 7'	CC failed mask
00005774	00000000	00000000		4151+	DS	2F	extracted PSW after test (has CC)
0000577C	FF			4152+	DC	X' FF'	extracted CC, if test failed
0000577D	E5C3C5D8	40404040		4153+	DC	CL8' VCEQ'	instruction name
00005788	00005800			4154+	DC	A(RE91)	address of v1 result
0000578C	00005810			4155+	DC	A(RE91+16)	address of v2 source
00005790	00005820			4156+	DC	A(RE91+32)	address of v3 source
00005794	00000010			4157+	DC	A(16)	result length
00005798	00005800			4158+REA91	DC	A(RE91)	result address
000057A0	00000000	00000000		4159+	DS	2FD	gap
000057A8	00000000	00000000					
000057B0	00000000	00000000		4160+V1091	DS	XL16	V1 output
000057B8	00000000	00000000					
000057C0	00000000	00000000		4161+	DS	2FD	gap
000057C8	00000000	00000000					
				4162+*			
000057D0				4163+X91	DS	0F	
000057D0	E310 5024 0014		00000024	4164+	LGF	R1, V2ADDR	load v2 source
000057D6	E761 0000 0806		00000000	4165+	VL	v22, 0(R1)	use v21 to test decoder
000057DC	E310 5028 0014		00000028	4166+	LGF	R1, V3ADDR	load v3 source
000057E2	E771 0000 0806		00000000	4167+	VL	v23, 0(R1)	use v22 to test decoder
000057E8	E756 7010 2EF8			4168+	VCEQ	V21, V22, V23, 2, 1	test instruction
000057EE	B98D 0020			4169+	EPSW	R2, R0	extract psw
000057F2	5020 500C		0000000C	4170+	ST	R2, CCPSW	to save CC
000057F6	E750 5048 080E		000057B0	4171+	VST	V21, V1091	save v1 output
000057FC	07FB			4172+	BR	R11	return
00005800				4173+RE91	DC	0F	V1 for this test
00005800				4174+	DROP	R5	
00005800	FFFFFFFF	FFFFFFFF		4175	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005808	FFFFFFFF	FFFFFFFF					
00005810	00110033	00550077		4176	DC	XL16' 0011003300550077 0022004400660008'	v2
00005818	00220044	00660008					
00005820	00110033	00550077		4177	DC	XL16' 0011003300550077 0022004400660008'	v3
00005828	00220044	00660008					
				4178			
				4179	VRR_B	VCEQ, 2, 0	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005830				4180+	DS	OFD	
00005830		00005830		4181+	USING	*, R5	base for test data and test routine
00005830	00005898			4182+T92	DC	A(X92)	address of test routine
00005834	005C			4183+	DC	H' 92'	test number
00005836	00			4184+	DC	X' 00'	
00005837	02			4185+	DC	HL1' 2'	m4 used
00005838	01			4186+	DC	HL1' 1'	m5 used
00005839	00			4187+	DC	HL1' 0'	CC
0000583A	07			4188+	DC	HL1' 7'	CC failed mask
0000583C	00000000 00000000			4189+	DS	2F	extracted PSW after test (has CC)
00005844	FF			4190+	DC	X' FF'	extracted CC, if test failed
00005845	E5C3C5D8 40404040			4191+	DC	CL8' VCEQ'	instruction name
00005850	000058C8			4192+	DC	A(RE92)	address of v1 result
00005854	000058D8			4193+	DC	A(RE92+16)	address of v2 source
00005858	000058E8			4194+	DC	A(RE92+32)	address of v3 source
0000585C	00000010			4195+	DC	A(16)	result length
00005860	000058C8			4196+REA92	DC	A(RE92)	result address
00005868	00000000 00000000			4197+	DS	2FD	gap
00005870	00000000 00000000						
00005878	00000000 00000000			4198+V1092	DS	XL16	V1 output
00005880	00000000 00000000						
00005888	00000000 00000000			4199+	DS	2FD	gap
00005890	00000000 00000000						
00005898				4200+*			
00005898	E310 5024 0014		00000024	4201+X92	DS	0F	
0000589E	E761 0000 0806		00000000	4202+	LGF	R1, V2ADDR	load v2 source
000058A4	E310 5028 0014		00000028	4203+	VL	v22, 0(R1)	use v21 to test decoder
000058AA	E771 0000 0806		00000000	4204+	LGF	R1, V3ADDR	load v3 source
000058B0	E756 7010 2EF8			4205+	VL	v23, 0(R1)	use v22 to test decoder
000058B6	B98D 0020			4206+	VCEQ	V21, V22, V23, 2, 1	test instruction
000058BA	5020 500C		0000000C	4207+	EPSW	R2, R0	extract psw
000058BE	E750 5048 080E		00005878	4208+	ST	R2, CCPSW	to save CC
000058C4	07FB			4209+	VST	V21, V1092	save v1 output
000058C8				4210+	BR	R11	return
000058C8				4211+RE92	DC	0F	V1 for this test
000058C8				4212+	DROP	R5	
000058C8	FFFFFFFF FFFFFFFF			4213	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000058D0	FFFFFFFF FFFFFFFF						
000058D8	FFFEFFFD FFFCFFFB			4214	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
000058E0	FFFAFFF9 FFF8FFF7						
000058E8	FFFEFFFD FFFCFFFB			4215	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
000058F0	FFFAFFF9 FFF8FFF7						
000058F8				4216			
000058F8		000058F8		4217	VRR_B	VCEQ, 2, 1	
000058F8	00005960			4218+	DS	OFD	
000058FC	005D			4219+	USING	*, R5	base for test data and test routine
000058FE	00			4220+T93	DC	A(X93)	address of test routine
000058FF	02			4221+	DC	H' 93'	test number
00005900	01			4222+	DC	X' 00'	
00005901	01			4223+	DC	HL1' 2'	m4 used
00005902	0B			4224+	DC	HL1' 1'	m5 used
00005904	00000000 00000000			4225+	DC	HL1' 1'	CC
0000590C	FF			4226+	DC	HL1' 11'	CC failed mask
0000590D	E5C3C5D8 40404040			4227+	DS	2F	extracted PSW after test (has CC)
				4228+	DC	X' FF'	extracted CC, if test failed
				4229+	DC	CL8' VCEQ'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005918	00005990			4230+	DC	A(RE93)	address of v1 result
0000591C	000059A0			4231+	DC	A(RE93+16)	address of v2 source
00005920	000059B0			4232+	DC	A(RE93+32)	address of v3 source
00005924	00000010			4233+	DC	A(16)	result length
00005928	00005990			4234+REA93	DC	A(RE93)	result address
00005930	00000000 00000000			4235+	DS	2FD	gap
00005938	00000000 00000000						
00005940	00000000 00000000			4236+V1093	DS	XL16	V1 output
00005948	00000000 00000000						
00005950	00000000 00000000			4237+	DS	2FD	gap
00005958	00000000 00000000						
00005960				4238+*			
00005960	E310 5024 0014		00000024	4239+X93	DS	0F	
00005966	E761 0000 0806		00000000	4240+	LGF	R1, V2ADDR	load v2 source
0000596C	E310 5028 0014		00000028	4241+	VL	v22, 0(R1)	use v21 to test decoder
00005972	E771 0000 0806		00000000	4242+	LGF	R1, V3ADDR	load v3 source
00005978	E756 7010 2EF8			4243+	VL	v23, 0(R1)	use v22 to test decoder
0000597E	B98D 0020			4244+	VCEQ	V21, V22, V23, 2, 1	test instruction
00005982	5020 500C		0000000C	4245+	EPSW	R2, R0	extract psw
00005986	E750 5048 080E		00005940	4246+	ST	R2, CCPSW	to save CC
0000598C	07FB			4247+	VST	V21, V1093	save v1 output
00005990				4248+	BR	R11	return
00005990				4249+RE93	DC	0F	V1 for this test
00005990	FFFFFFFF 00000000			4250+	DROP	R5	
00005998	FFFFFFFF FFFFFFFF			4251	DC	XL16' FFFFFFFF00000000 FFFFFFFF'	result
000059A0	00010203 04050607			4252	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2
000059A8	08090A0B 0C0DFE0F						
000059B0	00010203 00550077			4253	DC	XL16' 0001020300550077 08090A0B0C0DFE0F'	v3
000059B8	08090A0B 0C0DFE0F						
000059C0				4254			
000059C0		000059C0		4255	VRR_B	VCEQ, 2, 1	
000059C0	00005A28			4256+	DS	0FD	
000059C4	005E			4257+	USING	*, R5	base for test data and test routine
000059C6	00			4258+T94	DC	A(X94)	address of test routine
000059C7	02			4259+	DC	H' 94'	test number
000059C8	01			4260+	DC	X' 00'	
000059C9	01			4261+	DC	HL1' 2'	m4 used
000059CA	0B			4262+	DC	HL1' 1'	m5 used
000059CC	00000000 00000000			4263+	DC	HL1' 1'	CC
000059D4	FF			4264+	DC	HL1' 11'	CC failed mask
000059D5	E5C3C5D8 40404040			4265+	DS	2F	extracted PSW after test (has CC)
000059E0	00005A58			4266+	DC	X' FF'	extracted CC, if test failed
000059E4	00005A68			4267+	DC	CL8' VCEQ'	instruction name
000059E8	00005A78			4268+	DC	A(RE94)	address of v1 result
000059EC	00000010			4269+	DC	A(RE94+16)	address of v2 source
000059F0	00005A58			4270+	DC	A(RE94+32)	address of v3 source
000059F8	00000000 00000000			4271+	DC	A(16)	result length
00005A00	00000000 00000000			4272+REA94	DC	A(RE94)	result address
00005A08	00000000 00000000			4273+	DS	2FD	gap
00005A10	00000000 00000000						
00005A18	00000000 00000000			4274+V1094	DS	XL16	V1 output
00005A20	00000000 00000000			4275+	DS	2FD	gap
				4276+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005A28				4277+X94	DS	0F	
00005A28	E310 5024 0014		00000024	4278+	LGF	R1, V2ADDR	load v2 source
00005A2E	E761 0000 0806		00000000	4279+	VL	v22, 0(R1)	use v21 to test decoder
00005A34	E310 5028 0014		00000028	4280+	LGF	R1, V3ADDR	load v3 source
00005A3A	E771 0000 0806		00000000	4281+	VL	v23, 0(R1)	use v22 to test decoder
00005A40	E756 7010 2EF8			4282+	VCEQ	V21, V22, V23, 2, 1	test instruction
00005A46	B98D 0020			4283+	EPSW	R2, R0	extract psw
00005A4A	5020 500C		0000000C	4284+	ST	R2, CCPSW	to save CC
00005A4E	E750 5048 080E		00005A08	4285+	VST	V21, V1094	save v1 output
00005A54	07FB			4286+	BR	R11	return
00005A58				4287+RE94	DC	0F	V1 for this test
00005A58				4288+	DROP	R5	
00005A58	FFFFFFFF FFFFFFFF			4289	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result
00005A60	00000000 FFFFFFFF						
00005A68	08090A0B 0C0DFE0F			4290	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2
00005A70	00010203 04050607						
00005A78	08090A0B 0C0DFE0F			4291	DC	XL16' 08090A0B0C0DFE0F 0011003304050607'	v3
00005A80	00110033 04050607						
				4292			
				4293	VRR_B	VCEQ, 2, 3	
00005A88				4294+	DS	0FD	
00005A88		00005A88		4295+	USING	*, R5	base for test data and test routine
00005A88	00005AF0			4296+T95	DC	A(X95)	address of test routine
00005A8C	005F			4297+	DC	H' 95'	test number
00005A8E	00			4298+	DC	X' 00'	
00005A8F	02			4299+	DC	HL1' 2'	m4 used
00005A90	01			4300+	DC	HL1' 1'	m5 used
00005A91	03			4301+	DC	HL1' 3'	CC
00005A92	0E			4302+	DC	HL1' 14'	CC failed mask
00005A94	00000000 00000000			4303+	DS	2F	extracted PSW after test (has CC)
00005A9C	FF			4304+	DC	X' FF'	extracted CC, if test failed
00005A9D	E5C3C5D8 40404040			4305+	DC	CL8' VCEQ'	instruction name
00005AA8	00005B20			4306+	DC	A(RE95)	address of v1 result
00005AAC	00005B30			4307+	DC	A(RE95+16)	address of v2 source
00005AB0	00005B40			4308+	DC	A(RE95+32)	address of v3 source
00005AB4	00000010			4309+	DC	A(16)	result length
00005AB8	00005B20			4310+REA95	DC	A(RE95)	result address
00005AC0	00000000 00000000			4311+	DS	2FD	gap
00005AC8	00000000 00000000						
00005AD0	00000000 00000000			4312+V1095	DS	XL16	V1 output
00005AD8	00000000 00000000						
00005AE0	00000000 00000000			4313+	DS	2FD	gap
00005AE8	00000000 00000000						
				4314+*			
00005AF0				4315+X95	DS	0F	
00005AF0	E310 5024 0014		00000024	4316+	LGF	R1, V2ADDR	load v2 source
00005AF6	E761 0000 0806		00000000	4317+	VL	v22, 0(R1)	use v21 to test decoder
00005AFC	E310 5028 0014		00000028	4318+	LGF	R1, V3ADDR	load v3 source
00005B02	E771 0000 0806		00000000	4319+	VL	v23, 0(R1)	use v22 to test decoder
00005B08	E756 7010 2EF8			4320+	VCEQ	V21, V22, V23, 2, 1	test instruction
00005B0E	B98D 0020			4321+	EPSW	R2, R0	extract psw
00005B12	5020 500C		0000000C	4322+	ST	R2, CCPSW	to save CC
00005B16	E750 5048 080E		00005AD0	4323+	VST	V21, V1095	save v1 output
00005B1C	07FB			4324+	BR	R11	return
00005B20				4325+RE95	DC	0F	V1 for this test
00005B20				4326+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005B20	00000000 00000000			4327	DC	XL16' 0000000000000000 0000000000000000'	result
00005B28	00000000 00000000						
00005B30	01110133 01550177			4328	DC	XL16' 0111013301550177 019901BB01DD01FF'	v2
00005B38	019901BB 01DD01FF						
00005B40	00010203 04050607			4329	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00005B48	08090A0B 0C0D0E0F						
				4330			
				4331	VRR_B	VCEQ, 2, 3	
00005B50				4332+	DS	0FD	
00005B50		00005B50		4333+	USING	*, R5	base for test data and test routine
00005B50	00005BB8			4334+T96	DC	A(X96)	address of test routine
00005B54	0060			4335+	DC	H' 96'	test number
00005B56	00			4336+	DC	X' 00'	
00005B57	02			4337+	DC	HL1' 2'	m4 used
00005B58	01			4338+	DC	HL1' 1'	m5 used
00005B59	03			4339+	DC	HL1' 3'	CC
00005B5A	0E			4340+	DC	HL1' 14'	CC failed mask
00005B5C	00000000 00000000			4341+	DS	2F	extracted PSW after test (has CC)
00005B64	FF			4342+	DC	X' FF'	extracted CC, if test failed
00005B65	E5C3C5D8 40404040			4343+	DC	CL8' VCEQ'	instruction name
00005B70	00005BE8			4344+	DC	A(RE96)	address of v1 result
00005B74	00005BF8			4345+	DC	A(RE96+16)	address of v2 source
00005B78	00005C08			4346+	DC	A(RE96+32)	address of v3 source
00005B7C	00000010			4347+	DC	A(16)	result length
00005B80	00005BE8			4348+REA96	DC	A(RE96)	result address
00005B88	00000000 00000000			4349+	DS	2FD	gap
00005B90	00000000 00000000						
00005B98	00000000 00000000			4350+V1096	DS	XL16	V1 output
00005BA0	00000000 00000000						
00005BA8	00000000 00000000			4351+	DS	2FD	gap
00005BB0	00000000 00000000						
				4352+*			
00005BB8				4353+X96	DS	0F	
00005BB8	E310 5024 0014		00000024	4354+	LGF	R1, V2ADDR	load v2 source
00005BBE	E761 0000 0806		00000000	4355+	VL	v22, 0(R1)	use v21 to test decoder
00005BC4	E310 5028 0014		00000028	4356+	LGF	R1, V3ADDR	load v3 source
00005BCA	E771 0000 0806		00000000	4357+	VL	v23, 0(R1)	use v22 to test decoder
00005BD0	E756 7010 2EF8			4358+	VCEQ	V21, V22, V23, 2, 1	test instruction
00005BD6	B98D 0020			4359+	EPSW	R2, R0	extract psw
00005BDA	5020 500C		0000000C	4360+	ST	R2, CCPSW	to save CC
00005BDE	E750 5048 080E		00005B98	4361+	VST	V21, V1096	save v1 output
00005BE4	07FB			4362+	BR	R11	return
00005BE8				4363+RE96	DC	0F	V1 for this test
00005BE8				4364+	DROP	R5	
00005BE8	00000000 00000000			4365	DC	XL16' 0000000000000000 0000000000000000'	result
00005BF0	00000000 00000000						
00005BF8	00010203 04050607			4366	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00005C00	08090A0B 0C0D0E0F						
00005C08	01110133 01550177			4367	DC	XL16' 0111013301550177 019901BB01DD01FF'	v3
00005C10	019901BB 01DD01FF						
				4368			
				4369 *Doubleword			
				4370	VRR_B	VCEQ, 3, 0	
00005C18				4371+	DS	0FD	
00005C18		00005C18		4372+	USING	*, R5	base for test data and test routine
00005C18	00005C80			4373+T97	DC	A(X97)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005C1C	0061			4374+	DC	H' 97'	test number
00005C1E	00			4375+	DC	X' 00'	
00005C1F	03			4376+	DC	HL1' 3'	m4 used
00005C20	01			4377+	DC	HL1' 1'	m5 used
00005C21	00			4378+	DC	HL1' 0'	CC
00005C22	07			4379+	DC	HL1' 7'	CC failed mask
00005C24	00000000 00000000			4380+	DS	2F	extracted PSW after test (has CC)
00005C2C	FF			4381+	DC	X' FF'	extracted CC, if test failed
00005C2D	E5C3C5D8 40404040			4382+	DC	CL8' VCEQ'	instruction name
00005C38	00005CB0			4383+	DC	A(RE97)	address of v1 result
00005C3C	00005CC0			4384+	DC	A(RE97+16)	address of v2 source
00005C40	00005CD0			4385+	DC	A(RE97+32)	address of v3 source
00005C44	00000010			4386+	DC	A(16)	result length
00005C48	00005CB0			4387+REA97	DC	A(RE97)	result address
00005C50	00000000 00000000			4388+	DS	2FD	gap
00005C58	00000000 00000000						
00005C60	00000000 00000000			4389+V1097	DS	XL16	V1 output
00005C68	00000000 00000000						
00005C70	00000000 00000000			4390+	DS	2FD	gap
00005C78	00000000 00000000						
00005C80				4391+*			
00005C80	E310 5024 0014		00000024	4392+X97	DS	0F	
00005C86	E761 0000 0806		00000000	4393+	LGF	R1, V2ADDR	load v2 source
00005C8C	E310 5028 0014		00000028	4394+	VL	v22, 0(R1)	use v21 to test decoder
00005C92	E771 0000 0806		00000000	4395+	LGF	R1, V3ADDR	load v3 source
00005C98	E756 7010 3EF8		00000000	4396+	VL	v23, 0(R1)	use v22 to test decoder
00005C9E	B98D 0020			4397+	VCEQ	V21, V22, V23, 3, 1	test instruction
00005CA2	5020 500C		0000000C	4398+	EPSW	R2, R0	extract psw
00005CA6	E750 5048 080E		00005C60	4399+	ST	R2, CCPSW	to save CC
00005CAC	07FB			4400+	VST	V21, V1097	save v1 output
00005CB0				4401+	BR	R11	return
00005CB0				4402+RE97	DC	0F	V1 for this test
00005CB0	FFFFFFFF FFFFFFFF			4403+	DROP	R5	
00005CB8	FFFFFFFF FFFFFFFF			4404	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005CC0	00110033 00550077			4405	DC	XL16' 0011003300550077 0022004400660008'	v2
00005CC8	00220044 00660008						
00005CD0	00110033 00550077			4406	DC	XL16' 0011003300550077 0022004400660008'	v3
00005CD8	00220044 00660008						
00005CE0				4407			
00005CE0		00005CE0		4408	VRR_B	VCEQ, 3, 0	
00005CE0	00005D48			4409+	DS	0FD	
00005CE4	0062			4410+	USING	*, R5	base for test data and test routine
00005CE6	00			4411+T98	DC	A(X98)	address of test routine
00005CE7	03			4412+	DC	H' 98'	test number
00005CE8	01			4413+	DC	X' 00'	
00005CE9	00			4414+	DC	HL1' 3'	m4 used
00005CEA	07			4415+	DC	HL1' 1'	m5 used
00005CEC	00000000 00000000			4416+	DC	HL1' 0'	CC
00005CF4	FF			4417+	DC	HL1' 7'	CC failed mask
00005CF5	E5C3C5D8 40404040			4418+	DS	2F	extracted PSW after test (has CC)
00005D00	00005D78			4419+	DC	X' FF'	extracted CC, if test failed
00005D04	00005D88			4420+	DC	CL8' VCEQ'	instruction name
00005D08	00005D98			4421+	DC	A(RE98)	address of v1 result
				4422+	DC	A(RE98+16)	address of v2 source
				4423+	DC	A(RE98+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005D0C	00000010			4424+	DC	A(16)	result length
00005D10	00005D78			4425+REA98	DC	A(RE98)	result address
00005D18	00000000 00000000			4426+	DS	2FD	gap
00005D20	00000000 00000000						
00005D28	00000000 00000000			4427+V1098	DS	XL16	V1 output
00005D30	00000000 00000000						
00005D38	00000000 00000000			4428+	DS	2FD	gap
00005D40	00000000 00000000						
				4429+*			
00005D48				4430+X98	DS	0F	
00005D48	E310 5024 0014		00000024	4431+	LGF	R1, V2ADDR	load v2 source
00005D4E	E761 0000 0806		00000000	4432+	VL	v22, 0(R1)	use v21 to test decoder
00005D54	E310 5028 0014		00000028	4433+	LGF	R1, V3ADDR	load v3 source
00005D5A	E771 0000 0806		00000000	4434+	VL	v23, 0(R1)	use v22 to test decoder
00005D60	E756 7010 3EF8			4435+	VCEQ	V21, V22, V23, 3, 1	test instruction
00005D66	B98D 0020			4436+	EPSW	R2, R0	extract psw
00005D6A	5020 500C		0000000C	4437+	ST	R2, CCPSW	to save CC
00005D6E	E750 5048 080E		00005D28	4438+	VST	V21, V1098	save v1 output
00005D74	07FB			4439+	BR	R11	return
00005D78				4440+RE98	DC	0F	V1 for this test
00005D78				4441+	DROP	R5	
00005D78	FFFFFFFF FFFFFFFF			4442	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00005D80	FFFFFFFF FFFFFFFF						
00005D88	FFFEFFFD FFFCFFFB			4443	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00005D90	FFFAFFF9 FFF8FFF7						
00005D98	FFFEFFFD FFFCFFFB			4444	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00005DA0	FFFAFFF9 FFF8FFF7						
				4445			
				4446	VRR_B	VCEQ, 3, 1	
00005DA8				4447+	DS	0FD	
00005DA8		00005DA8		4448+	USING	*, R5	base for test data and test routine
00005DA8	00005E10			4449+T99	DC	A(X99)	address of test routine
00005DAC	0063			4450+	DC	H' 99'	test number
00005DAE	00			4451+	DC	X' 00'	
00005DAF	03			4452+	DC	HL1' 3'	m4 used
00005DB0	01			4453+	DC	HL1' 1'	m5 used
00005DB1	01			4454+	DC	HL1' 1'	CC
00005DB2	0B			4455+	DC	HL1' 11'	CC failed mask
00005DB4	00000000 00000000			4456+	DS	2F	extracted PSW after test (has CC)
00005DBC	FF			4457+	DC	X' FF'	extracted CC, if test failed
00005DBD	E5C3C5D8 40404040			4458+	DC	CL8' VCEQ'	instruction name
00005DC8	00005E40			4459+	DC	A(RE99)	address of v1 result
00005DCC	00005E50			4460+	DC	A(RE99+16)	address of v2 source
00005DD0	00005E60			4461+	DC	A(RE99+32)	address of v3 source
00005DD4	00000010			4462+	DC	A(16)	result length
00005DD8	00005E40			4463+REA99	DC	A(RE99)	result address
00005DE0	00000000 00000000			4464+	DS	2FD	gap
00005DE8	00000000 00000000						
00005DF0	00000000 00000000			4465+V1099	DS	XL16	V1 output
00005DF8	00000000 00000000						
00005E00	00000000 00000000			4466+	DS	2FD	gap
00005E08	00000000 00000000						
				4467+*			
00005E10				4468+X99	DS	0F	
00005E10	E310 5024 0014		00000024	4469+	LGF	R1, V2ADDR	load v2 source
00005E16	E761 0000 0806		00000000	4470+	VL	v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00005E1C	E310 5028 0014		00000028	4471+	LGF	R1, V3ADDR	load v3 source	
00005E22	E771 0000 0806		00000000	4472+	VL	v23, 0(R1)	use v22 to test decoder	
00005E28	E756 7010 3EF8			4473+	VCEQ	V21, V22, V23, 3, 1	test instruction	
00005E2E	B98D 0020			4474+	EPSW	R2, R0	extract psw	
00005E32	5020 500C		0000000C	4475+	ST	R2, CCPSW	to save CC	
00005E36	E750 5048 080E		00005DF0	4476+	VST	V21, V1099	save v1 output	
00005E3C	07FB			4477+	BR	R11	return	
00005E40				4478+RE99	DC	0F	V1 for this test	
00005E40				4479+	DROP	R5		
00005E40	00000000 00000000			4480	DC	XL16' 0000000000000000 0000000000000000	result t	
00005E48	FFFFFFFF FFFFFFFF							
00005E50	00010203 04050607			4481	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'	v2	
00005E58	08090A0B 0C0DFE0F							
00005E60	00110033 00550077			4482	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v3	
00005E68	08090A0B 0C0DFE0F							
				4483				
00005E70				4484	VRR_B	VCEQ, 3, 1		
00005E70		00005E70		4485+	DS	0FD		
00005E70	00005ED8			4486+	USING	*, R5	base for test data and test routine	
00005E74	0064			4487+T100	DC	A(X100)	address of test routine	
00005E76	00			4488+	DC	H' 100'	test number	
00005E76	00			4489+	DC	X' 00'		
00005E77	03			4490+	DC	HL1' 3'	m4 used	
00005E78	01			4491+	DC	HL1' 1'	m5 used	
00005E79	01			4492+	DC	HL1' 1'	CC	
00005E7A	0B			4493+	DC	HL1' 11'	CC failed mask	
00005E7C	00000000 00000000			4494+	DS	2F	extracted PSW after test (has CC)	
00005E84	FF			4495+	DC	X' FF'	extracted CC, if test failed	
00005E85	E5C3C5D8 40404040			4496+	DC	CL8' VCEQ'	instruction name	
00005E90	00005F08			4497+	DC	A(RE100)	address of v1 result	
00005E94	00005F18			4498+	DC	A(RE100+16)	address of v2 source	
00005E98	00005F28			4499+	DC	A(RE100+32)	address of v3 source	
00005E9C	00000010			4500+	DC	A(16)	result length	
00005EA0	00005F08			4501+REA100	DC	A(RE100)	result address	
00005EA8	00000000 00000000			4502+	DS	2FD	gap	
00005EB0	00000000 00000000							
00005EB8	00000000 00000000			4503+V10100	DS	XL16	V1 output	
00005EC0	00000000 00000000							
00005EC8	00000000 00000000			4504+	DS	2FD	gap	
00005ED0	00000000 00000000							
				4505+*				
00005ED8				4506+X100	DS	0F		
00005ED8	E310 5024 0014		00000024	4507+	LGF	R1, V2ADDR	load v2 source	
00005EDE	E761 0000 0806		00000000	4508+	VL	v22, 0(R1)	use v21 to test decoder	
00005EE4	E310 5028 0014		00000028	4509+	LGF	R1, V3ADDR	load v3 source	
00005EEA	E771 0000 0806		00000000	4510+	VL	v23, 0(R1)	use v22 to test decoder	
00005EF0	E756 7010 3EF8			4511+	VCEQ	V21, V22, V23, 3, 1	test instruction	
00005EF6	B98D 0020			4512+	EPSW	R2, R0	extract psw	
00005EFA	5020 500C		0000000C	4513+	ST	R2, CCPSW	to save CC	
00005EFE	E750 5048 080E		00005EB8	4514+	VST	V21, V10100	save v1 output	
00005F04	07FB			4515+	BR	R11	return	
00005F08				4516+RE100	DC	0F	V1 for this test	
00005F08				4517+	DROP	R5		
00005F08	FFFFFFFF FFFFFFFF			4518	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result t	
00005F10	00000000 00000000							
00005F18	08090A0B 0C0DFE0F			4519	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v2	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00005F20	00010203 04050607							
00005F28	08090A0B 0C0DFE0F			4520	DC	XL16' 08090A0B0C0DFE0F	0011003300550077'	v3
00005F30	00110033 00550077							
				4521				
				4522	VRR_B	VCEQ, 3, 3		
00005F38				4523+	DS	0FD		
00005F38		00005F38		4524+	USING	*, R5		base for test data and test routine
00005F38	00005FA0			4525+T101	DC	A(X101)		address of test routine
00005F3C	0065			4526+	DC	H' 101'		test number
00005F3E	00			4527+	DC	X' 00'		
00005F3F	03			4528+	DC	HL1' 3'		m4 used
00005F40	01			4529+	DC	HL1' 1'		m5 used
00005F41	03			4530+	DC	HL1' 3'		CC
00005F42	0E			4531+	DC	HL1' 14'		CC failed mask
00005F44	00000000 00000000			4532+	DS	2F		extracted PSW after test (has CC)
00005F4C	FF			4533+	DC	X' FF'		extracted CC, if test failed
00005F4D	E5C3C5D8 40404040			4534+	DC	CL8' VCEQ'		instruction name
00005F58	00005FD0			4535+	DC	A(RE101)		address of v1 result
00005F5C	00005FE0			4536+	DC	A(RE101+16)		address of v2 source
00005F60	00005FF0			4537+	DC	A(RE101+32)		address of v3 source
00005F64	00000010			4538+	DC	A(16)		result length
00005F68	00005FD0			4539+REA101	DC	A(RE101)		result address
00005F70	00000000 00000000			4540+	DS	2FD		gap
00005F78	00000000 00000000							
00005F80	00000000 00000000			4541+V10101	DS	XL16		V1 output
00005F88	00000000 00000000							
00005F90	00000000 00000000			4542+	DS	2FD		gap
00005F98	00000000 00000000							
				4543+*				
00005FA0				4544+X101	DS	0F		
00005FA0	E310 5024 0014		00000024	4545+	LGF	R1, V2ADDR		load v2 source
00005FA6	E761 0000 0806		00000000	4546+	VL	v22, 0(R1)		use v21 to test decoder
00005FAC	E310 5028 0014		00000028	4547+	LGF	R1, V3ADDR		load v3 source
00005FB2	E771 0000 0806		00000000	4548+	VL	v23, 0(R1)		use v22 to test decoder
00005FB8	E756 7010 3EF8			4549+	VCEQ	V21, V22, V23, 3, 1		test instruction
00005FBE	B98D 0020			4550+	EPSW	R2, R0		extract psw
00005FC2	5020 500C		0000000C	4551+	ST	R2, CCPSW		to save CC
00005FC6	E750 5048 080E		00005F80	4552+	VST	V21, V10101		save v1 output
00005FCC	07FB			4553+	BR	R11		return
00005FD0				4554+RE101	DC	0F		V1 for this test
00005FD0				4555+	DROP	R5		
00005FD0	00000000 00000000			4556	DC	XL16' 0000000000000000 0000000000000000'		result t
00005FD8	00000000 00000000							
00005FE0	01110133 01550177			4557	DC	XL16' 0111013301550177 019901BB01DD01FF'		v2
00005FE8	019901BB 01DD01FF							
00005FF0	00010203 04050607			4558	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'		v3
00005FF8	08090A0B 0C0D0E0F							
				4559				
				4560	VRR_B	VCEQ, 3, 3		
00006000				4561+	DS	0FD		
00006000		00006000		4562+	USING	*, R5		base for test data and test routine
00006000	00006068			4563+T102	DC	A(X102)		address of test routine
00006004	0066			4564+	DC	H' 102'		test number
00006006	00			4565+	DC	X' 00'		
00006007	03			4566+	DC	HL1' 3'		m4 used
00006008	01			4567+	DC	HL1' 1'		m5 used

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00006009	03			4568+	DC	HL1' 3'
0000600A	0E			4569+	DC	HL1' 14'
0000600C	00000000 00000000			4570+	DS	2F
00006014	FF			4571+	DC	X' FF'
00006015	E5C3C5D8 40404040			4572+	DC	CL8' VCEQ'
00006020	00006098			4573+	DC	A(RE102)
00006024	000060A8			4574+	DC	A(RE102+16)
00006028	000060B8			4575+	DC	A(RE102+32)
0000602C	00000010			4576+	DC	A(16)
00006030	00006098			4577+REA102	DC	A(RE102)
00006038	00000000 00000000			4578+	DS	2FD
00006040	00000000 00000000					gap
00006048	00000000 00000000			4579+V10102	DS	XL16
00006050	00000000 00000000					V1 output
00006058	00000000 00000000			4580+	DS	2FD
00006060	00000000 00000000					gap
				4581+*		
00006068				4582+X102	DS	0F
00006068	E310 5024 0014		00000024	4583+	LGF	R1, V2ADDR
0000606E	E761 0000 0806		00000000	4584+	VL	v22, 0(R1)
00006074	E310 5028 0014		00000028	4585+	LGF	R1, V3ADDR
0000607A	E771 0000 0806		00000000	4586+	VL	v23, 0(R1)
00006080	E756 7010 3EF8			4587+	VCEQ	V21, V22, V23, 3, 1
00006086	B98D 0020			4588+	EPSW	R2, R0
0000608A	5020 500C		0000000C	4589+	ST	R2, CCPSW
0000608E	E750 5048 080E		00006048	4590+	VST	V21, V10102
00006094	07FB			4591+	BR	R11
00006098				4592+RE102	DC	0F
00006098				4593+	DROP	R5
00006098	00000000 00000000			4594	DC	XL16' 0000000000000000 0000000000000000'
000060A0	00000000 00000000					result t
000060A8	00010203 04050607			4595	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'
000060B0	08090A0B 0C0D0E0F					v2
000060B8	01110133 01550177			4596	DC	XL16' 0111013301550177 019901BB01DD01FF'
000060C0	019901BB 01DD01FF					v3
				4597		
				4598 *		-----
				4599 * VCHL		- Vector Compare High Logical
				4600 *		-----
				4601 *		cc=0: All elements high
				4602 *		cc=1: Some elements high
				4603 *		cc=3: No element high
				4604 *		-----
				4605 *		case - simple cc debug
				4606 *		-----
				4607 *		Byte
				4608	VRR_B	VCHL, 0, 0
000060C8				4609+	DS	0FD
000060C8		000060C8		4610+	USING	*, R5
000060C8	00006130			4611+T103	DC	A(X103)
000060CC	0067			4612+	DC	H' 103'
000060CE	00			4613+	DC	X' 00'
000060CF	00			4614+	DC	HL1' 0'
000060D0	01			4615+	DC	HL1' 1'
000060D1	00			4616+	DC	HL1' 0'
000060D2	07			4617+	DC	HL1' 7'
						CC
						CC failed mask

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000060D4	00000000 00000000			4618+	DS	2F	extracted PSW after test (has CC)
000060DC	FF			4619+	DC	X' FF'	extracted CC, if test failed
000060DD	E5C3C8D3 40404040			4620+	DC	CL8' VCHL'	instruction name
000060E8	00006160			4621+	DC	A(RE103)	address of v1 result
000060EC	00006170			4622+	DC	A(RE103+16)	address of v2 source
000060F0	00006180			4623+	DC	A(RE103+32)	address of v3 source
000060F4	00000010			4624+	DC	A(16)	result length
000060F8	00006160			4625+REA103	DC	A(RE103)	result address
00006100	00000000 00000000			4626+	DS	2FD	gap
00006108	00000000 00000000						
00006110	00000000 00000000			4627+V10103	DS	XL16	V1 output
00006118	00000000 00000000						
00006120	00000000 00000000			4628+	DS	2FD	gap
00006128	00000000 00000000						
				4629+*			
00006130				4630+X103	DS	0F	
00006130	E310 5024 0014		00000024	4631+	LGF	R1, V2ADDR	load v2 source
00006136	E761 0000 0806		00000000	4632+	VL	v22, 0(R1)	use v21 to test decoder
0000613C	E310 5028 0014		00000028	4633+	LGF	R1, V3ADDR	load v3 source
00006142	E771 0000 0806		00000000	4634+	VL	v23, 0(R1)	use v22 to test decoder
00006148	E756 7010 0EF9			4635+	VCHL	V21, V22, V23, 0, 1	test instruction
0000614E	B98D 0020			4636+	EPSW	R2, R0	extract psw
00006152	5020 500C		0000000C	4637+	ST	R2, CCPSW	to save CC
00006156	E750 5048 080E		00006110	4638+	VST	V21, V10103	save v1 output
0000615C	07FB			4639+	BR	R11	return
00006160				4640+RE103	DC	0F	V1 for this test
00006160				4641+	DROP	R5	
00006160	FFFFFFFF FFFFFFFF			4642	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00006168	FFFFFFFF FFFFFFFF						
00006170	FFFFFFFF FFFFFFFF			4643	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00006178	FFFFFFFF FFFFFFFF						
00006180	00000000 00000000			4644	DC	XL16' 0000000000000000 0000000000000000'	v3
00006188	00000000 00000000						
				4645			
				4646	VRR_B	VCHL, 0, 1	
00006190				4647+	DS	0FD	
00006190		00006190		4648+	USING	*, R5	base for test data and test routine
00006190	000061F8			4649+T104	DC	A(X104)	address of test routine
00006194	0068			4650+	DC	H' 104'	test number
00006196	00			4651+	DC	X' 00'	
00006197	00			4652+	DC	HL1' 0'	m4 used
00006198	01			4653+	DC	HL1' 1'	m5 used
00006199	01			4654+	DC	HL1' 1'	CC
0000619A	0B			4655+	DC	HL1' 11'	CC failed mask
0000619C	00000000 00000000			4656+	DS	2F	extracted PSW after test (has CC)
000061A4	FF			4657+	DC	X' FF'	extracted CC, if test failed
000061A5	E5C3C8D3 40404040			4658+	DC	CL8' VCHL'	instruction name
000061B0	00006228			4659+	DC	A(RE104)	address of v1 result
000061B4	00006238			4660+	DC	A(RE104+16)	address of v2 source
000061B8	00006248			4661+	DC	A(RE104+32)	address of v3 source
000061BC	00000010			4662+	DC	A(16)	result length
000061C0	00006228			4663+REA104	DC	A(RE104)	result address
000061C8	00000000 00000000			4664+	DS	2FD	gap
000061D0	00000000 00000000						
000061D8	00000000 00000000			4665+V10104	DS	XL16	V1 output
000061E0	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000061E8	00000000 00000000			4666+	DS	2FD	gap
000061F0	00000000 00000000						
000061F8				4667+*			
000061F8	E310 5024 0014		00000024	4668+X104	DS	0F	
000061FE	E761 0000 0806		00000000	4669+	LGF	R1, V2ADDR	load v2 source
00006204	E310 5028 0014		00000028	4670+	VL	v22, 0(R1)	use v21 to test decoder
0000620A	E771 0000 0806		00000000	4671+	LGF	R1, V3ADDR	load v3 source
00006210	E756 7010 0EF9			4672+	VL	v23, 0(R1)	use v22 to test decoder
00006216	B98D 0020			4673+	VCHL	V21, V22, V23, 0, 1	test instruction
0000621A	5020 500C		0000000C	4674+	EPSW	R2, R0	extract psw
0000621E	E750 5048 080E		000061D8	4675+	ST	R2, CCPSW	to save CC
00006224	07FB			4676+	VST	V21, V10104	save v1 output
00006228				4677+	BR	R11	return
00006228				4678+RE104	DC	0F	V1 for this test
00006228	00000000 00000000			4679+	DROP	R5	
00006230	FFFFFFFF 00000000			4680	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result
00006238	00000000 00000000			4681	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v2
00006240	8FFF8FFF 00000000						
00006248	00000000 00000000			4682	DC	XL16' 0000000000000000 0000000000000000'	v3
00006250	00000000 00000000						
00006258				4683			
00006258				4684	VRR_B	VCHL, 0, 3	
00006258		00006258		4685+	DS	0FD	
00006258	000062C0			4686+	USING	*, R5	base for test data and test routine
0000625C	0069			4687+T105	DC	A(X105)	address of test routine
0000625E	00			4688+	DC	H' 105'	test number
0000625F	00			4689+	DC	X' 00'	
00006260	01			4690+	DC	HL1' 0'	m4 used
00006261	03			4691+	DC	HL1' 1'	m5 used
00006262	0E			4692+	DC	HL1' 3'	CC
00006264	00000000 00000000			4693+	DC	HL1' 14'	CC failed mask
0000626C	FF			4694+	DS	2F	extracted PSW after test (has CC)
0000626D	E5C3C8D3 40404040			4695+	DC	X' FF'	extracted CC, if test failed
00006278	000062F0			4696+	DC	CL8' VCHL'	instruction name
0000627C	00006300			4697+	DC	A(RE105)	address of v1 result
00006280	00006310			4698+	DC	A(RE105+16)	address of v2 source
00006284	00000010			4699+	DC	A(RE105+32)	address of v3 source
00006288	000062F0			4700+	DC	A(16)	result length
00006290	00000000 00000000			4701+REA105	DC	A(RE105)	result address
00006298	00000000 00000000			4702+	DS	2FD	gap
000062A0	00000000 00000000			4703+V10105	DS	XL16	V1 output
000062A8	00000000 00000000						
000062B0	00000000 00000000			4704+	DS	2FD	gap
000062B8	00000000 00000000						
000062C0				4705+*			
000062C0	E310 5024 0014		00000024	4706+X105	DS	0F	
000062C6	E761 0000 0806		00000000	4707+	LGF	R1, V2ADDR	load v2 source
000062CC	E310 5028 0014		00000028	4708+	VL	v22, 0(R1)	use v21 to test decoder
000062D2	E771 0000 0806		00000000	4709+	LGF	R1, V3ADDR	load v3 source
000062D8	E756 7010 0EF9			4710+	VL	v23, 0(R1)	use v22 to test decoder
000062DE	B98D 0020			4711+	VCHL	V21, V22, V23, 0, 1	test instruction
000062E2	5020 500C		0000000C	4712+	EPSW	R2, R0	extract psw
000062E6	E750 5048 080E		000062A0	4713+	ST	R2, CCPSW	to save CC
				4714+	VST	V21, V10105	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000062EC	07FB			4715+	BR	R11	return
000062F0				4716+RE105	DC	0F	V1 for this test
000062F0				4717+	DROP	R5	
000062F0	00000000 00000000			4718	DC	XL16' 0000000000000000 0000000000000000'	result t
000062F8	00000000 00000000						
00006300	00000000 00000000			4719	DC	XL16' 0000000000000000 0000000000000000'	v2
00006308	00000000 00000000						
00006310	00000000 00000000			4720	DC	XL16' 0000000000000000 0000000000000000'	v3
00006318	00000000 00000000						
				4721			
				4722 *Halfword			
				4723	VRR_B	VCHL, 1, 0	
00006320				4724+	DS	0FD	
00006320		00006320		4725+	USING	*, R5	base for test data and test routine
00006320	00006388			4726+T106	DC	A(X106)	address of test routine
00006324	006A			4727+	DC	H' 106'	test number
00006326	00			4728+	DC	X' 00'	
00006327	01			4729+	DC	HL1' 1'	m4 used
00006328	01			4730+	DC	HL1' 1'	m5 used
00006329	00			4731+	DC	HL1' 0'	CC
0000632A	07			4732+	DC	HL1' 7'	CC failed mask
0000632C	00000000 00000000			4733+	DS	2F	extracted PSW after test (has CC)
00006334	FF			4734+	DC	X' FF'	extracted CC, if test failed
00006335	E5C3C8D3 40404040			4735+	DC	CL8' VCHL'	instruction name
00006340	000063B8			4736+	DC	A(RE106)	address of v1 result
00006344	000063C8			4737+	DC	A(RE106+16)	address of v2 source
00006348	000063D8			4738+	DC	A(RE106+32)	address of v3 source
0000634C	00000010			4739+	DC	A(16)	result length
00006350	000063B8			4740+REA106	DC	A(RE106)	result address
00006358	00000000 00000000			4741+	DS	2FD	gap
00006360	00000000 00000000						
00006368	00000000 00000000			4742+V10106	DS	XL16	V1 output
00006370	00000000 00000000						
00006378	00000000 00000000			4743+	DS	2FD	gap
00006380	00000000 00000000						
				4744+*			
00006388				4745+X106	DS	0F	
00006388	E310 5024 0014		00000024	4746+	LGF	R1, V2ADDR	load v2 source
0000638E	E761 0000 0806		00000000	4747+	VL	v22, 0(R1)	use v21 to test decoder
00006394	E310 5028 0014		00000028	4748+	LGF	R1, V3ADDR	load v3 source
0000639A	E771 0000 0806		00000000	4749+	VL	v23, 0(R1)	use v22 to test decoder
000063A0	E756 7010 1EF9			4750+	VCHL	V21, V22, V23, 1, 1	test instruction
000063A6	B98D 0020			4751+	EPSW	R2, R0	extract psw
000063AA	5020 500C		0000000C	4752+	ST	R2, CCPSW	to save CC
000063AE	E750 5048 080E		00006368	4753+	VST	V21, V10106	save v1 output
000063B4	07FB			4754+	BR	R11	return
000063B8				4755+RE106	DC	0F	V1 for this test
000063B8				4756+	DROP	R5	
000063B8	FFFFFFFF FFFFFFFF			4757	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000063C0	FFFFFFFF FFFFFFFF						
000063C8	FFFFFFFF FFFFFFFF			4758	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
000063D0	FFFFFFFF FFFFFFFF						
000063D8	00000000 00000000			4759	DC	XL16' 0000000000000000 0000000000000000'	v3
000063E0	00000000 00000000						
				4760			
				4761	VRR_B	VCHL, 1, 1	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000063E8				4762+	DS	0FD	
000063E8		000063E8		4763+	USING	*, R5	base for test data and test routine
000063E8	00006450			4764+T107	DC	A(X107)	address of test routine
000063EC	006B			4765+	DC	H' 107'	test number
000063EE	00			4766+	DC	X' 00'	
000063EF	01			4767+	DC	HL1' 1'	m4 used
000063F0	01			4768+	DC	HL1' 1'	m5 used
000063F1	01			4769+	DC	HL1' 1'	CC
000063F2	0B			4770+	DC	HL1' 11'	CC failed mask
000063F4	00000000 00000000			4771+	DS	2F	extracted PSW after test (has CC)
000063FC	FF			4772+	DC	X' FF'	extracted CC, if test failed
000063FD	E5C3C8D3 40404040			4773+	DC	CL8' VCHL'	instruction name
00006408	00006480			4774+	DC	A(RE107)	address of v1 result
0000640C	00006490			4775+	DC	A(RE107+16)	address of v2 source
00006410	000064A0			4776+	DC	A(RE107+32)	address of v3 source
00006414	00000010			4777+	DC	A(16)	result length
00006418	00006480			4778+REA107	DC	A(RE107)	result address
00006420	00000000 00000000			4779+	DS	2FD	gap
00006428	00000000 00000000						
00006430	00000000 00000000			4780+V10107	DS	XL16	V1 output
00006438	00000000 00000000						
00006440	00000000 00000000			4781+	DS	2FD	gap
00006448	00000000 00000000						
00006450				4782+*			
00006450	E310 5024 0014			4783+X107	DS	0F	
00006456	E761 0000 0806		00000024	4784+	LGF	R1, V2ADDR	load v2 source
0000645C	E310 5028 0014		00000000	4785+	VL	v22, 0(R1)	use v21 to test decoder
00006462	E771 0000 0806		00000028	4786+	LGF	R1, V3ADDR	load v3 source
00006468	E756 7010 1EF9		00000000	4787+	VL	v23, 0(R1)	use v22 to test decoder
0000646E	B98D 0020			4788+	VCHL	V21, V22, V23, 1, 1	test instruction
00006472	5020 500C			4789+	EPSW	R2, R0	extract psw
00006476	E750 5048 080E		0000000C	4790+	ST	R2, CCPSW	to save CC
0000647C	07FB		00006430	4791+	VST	V21, V10107	save v1 output
00006480				4792+	BR	R11	return
00006480				4793+RE107	DC	0F	V1 for this test
00006480				4794+	DROP	R5	
00006480	00000000 00000000			4795	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result
00006488	FFFFFFFF 00000000						
00006490	00000000 00000000			4796	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00006498	8FFF8FFF 00000000						
000064A0	00000000 00000000			4797	DC	XL16' 0000000000000000 0000000000000000'	v2
000064A8	00000000 00000000						
000064B0				4798			
000064B0				4799	VRR_B	VCHL, 1, 3	
000064B0	00006518	000064B0		4800+	DS	0FD	
000064B0				4801+	USING	*, R5	base for test data and test routine
000064B4	006C			4802+T108	DC	A(X108)	address of test routine
000064B6	00			4803+	DC	H' 108'	test number
000064B7	01			4804+	DC	X' 00'	
000064B8	01			4805+	DC	HL1' 1'	m4 used
000064B8	01			4806+	DC	HL1' 1'	m5 used
000064B9	03			4807+	DC	HL1' 3'	CC
000064BA	0E			4808+	DC	HL1' 14'	CC failed mask
000064BC	00000000 00000000			4809+	DS	2F	extracted PSW after test (has CC)
000064C4	FF			4810+	DC	X' FF'	extracted CC, if test failed
000064C5	E5C3C8D3 40404040			4811+	DC	CL8' VCHL'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000064D0	00006548			4812+	DC	A(RE108)	address of v1 result
000064D4	00006558			4813+	DC	A(RE108+16)	address of v2 source
000064D8	00006568			4814+	DC	A(RE108+32)	address of v3 source
000064DC	00000010			4815+	DC	A(16)	result length
000064E0	00006548			4816+REA108	DC	A(RE108)	result address
000064E8	00000000 00000000			4817+	DS	2FD	gap
000064F0	00000000 00000000						
000064F8	00000000 00000000			4818+V10108	DS	XL16	V1 output
00006500	00000000 00000000						
00006508	00000000 00000000			4819+	DS	2FD	gap
00006510	00000000 00000000						
00006518				4820+*			
00006518	E310 5024 0014		00000024	4821+X108	DS	0F	
0000651E	E761 0000 0806		00000000	4822+	LGF	R1, V2ADDR	load v2 source
00006524	E310 5028 0014		00000028	4823+	VL	v22, 0(R1)	use v21 to test decoder
0000652A	E771 0000 0806		00000000	4824+	LGF	R1, V3ADDR	load v3 source
00006530	E756 7010 1EF9			4825+	VL	v23, 0(R1)	use v22 to test decoder
00006536	B98D 0020			4826+	VCHL	V21, V22, V23, 1, 1	test instruction
0000653A	5020 500C		0000000C	4827+	EPSW	R2, R0	extract psw
0000653E	E750 5048 080E		000064F8	4828+	ST	R2, CCPSW	to save CC
00006544	07FB			4829+	VST	V21, V10108	save v1 output
00006548				4830+	BR	R11	return
00006548				4831+RE108	DC	0F	V1 for this test
00006548				4832+	DROP	R5	
00006548	00000000 00000000			4833	DC	XL16' 0000000000000000 0000000000000000'	result
00006550	00000000 00000000						
00006558	00000000 00000000			4834	DC	XL16' 0000000000000000 0000000000000000'	v2
00006560	00000000 00000000						
00006568	00000000 00000000			4835	DC	XL16' 0000000000000000 0000000000000000'	v3
00006570	00000000 00000000						
				4836			
				4837 *Word			
				4838	VRR_B	VCHL, 2, 0	
00006578				4839+	DS	0FD	
00006578		00006578		4840+	USING	*, R5	base for test data and test routine
00006578	000065E0			4841+T109	DC	A(X109)	address of test routine
0000657C	006D			4842+	DC	H' 109'	test number
0000657E	00			4843+	DC	X' 00'	
0000657F	02			4844+	DC	HL1' 2'	m4 used
00006580	01			4845+	DC	HL1' 1'	m5 used
00006581	00			4846+	DC	HL1' 0'	CC
00006582	07			4847+	DC	HL1' 7'	CC failed mask
00006584	00000000 00000000			4848+	DS	2F	extracted PSW after test (has CC)
0000658C	FF			4849+	DC	X' FF'	extracted CC, if test failed
0000658D	E5C3C8D3 40404040			4850+	DC	CL8' VCHL'	instruction name
00006598	00006610			4851+	DC	A(RE109)	address of v1 result
0000659C	00006620			4852+	DC	A(RE109+16)	address of v2 source
000065A0	00006630			4853+	DC	A(RE109+32)	address of v3 source
000065A4	00000010			4854+	DC	A(16)	result length
000065A8	00006610			4855+REA109	DC	A(RE109)	result address
000065B0	00000000 00000000			4856+	DS	2FD	gap
000065B8	00000000 00000000						
000065C0	00000000 00000000			4857+V10109	DS	XL16	V1 output
000065C8	00000000 00000000						
000065D0	00000000 00000000			4858+	DS	2FD	gap
000065D8	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				4859+*			
000065E0				4860+X109	DS	0F	
000065E0	E310 5024 0014		00000024	4861+	LGF	R1, V2ADDR	load v2 source
000065E6	E761 0000 0806		00000000	4862+	VL	v22, 0(R1)	use v21 to test decoder
000065EC	E310 5028 0014		00000028	4863+	LGF	R1, V3ADDR	load v3 source
000065F2	E771 0000 0806		00000000	4864+	VL	v23, 0(R1)	use v22 to test decoder
000065F8	E756 7010 2EF9			4865+	VCHL	V21, V22, V23, 2, 1	test instruction
000065FE	B98D 0020			4866+	EPSW	R2, R0	extract psw
00006602	5020 500C		0000000C	4867+	ST	R2, CCPSW	to save CC
00006606	E750 5048 080E		000065C0	4868+	VST	V21, V10109	save v1 output
0000660C	07FB			4869+	BR	R11	return
00006610				4870+RE109	DC	0F	V1 for this test
00006610				4871+	DROP	R5	
00006610	FFFFFFFF FFFFFFFF			4872	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00006618	FFFFFFFF FFFFFFFF						
00006620	FFFFFFFF FFFFFFFF			4873	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v2
00006628	FFFFFFFF FFFFFFFF						
00006630	00000000 00000000			4874	DC	XL16' 0000000000000000 0000000000000000'	v3
00006638	00000000 00000000						
				4875			
00006640				4876	VRR_B	VCHL, 2, 1	
00006640		00006640		4877+	DS	0FD	
00006640	000066A8			4878+	USING	*, R5	base for test data and test routine
00006644	006E			4879+T110	DC	A(X110)	address of test routine
00006646	00			4880+	DC	H' 110'	test number
00006647	02			4881+	DC	X' 00'	
00006648	01			4882+	DC	HL1' 2'	m4 used
00006648	01			4883+	DC	HL1' 1'	m5 used
00006649	01			4884+	DC	HL1' 1'	CC
0000664A	0B			4885+	DC	HL1' 11'	CC failed mask
0000664C	00000000 00000000			4886+	DS	2F	extracted PSW after test (has CC)
00006654	FF			4887+	DC	X' FF'	extracted CC, if test failed
00006655	E5C3C8D3 40404040			4888+	DC	CL8' VCHL'	instruction name
00006660	000066D8			4889+	DC	A(RE110)	address of v1 result
00006664	000066E8			4890+	DC	A(RE110+16)	address of v2 source
00006668	000066F8			4891+	DC	A(RE110+32)	address of v3 source
0000666C	00000010			4892+	DC	A(16)	result length
00006670	000066D8			4893+REA110	DC	A(RE110)	result address
00006678	00000000 00000000			4894+	DS	2FD	gap
00006680	00000000 00000000						
00006688	00000000 00000000			4895+V10110	DS	XL16	V1 output
00006690	00000000 00000000						
00006698	00000000 00000000			4896+	DS	2FD	gap
000066A0	00000000 00000000						
				4897+*			
000066A8				4898+X110	DS	0F	
000066A8	E310 5024 0014		00000024	4899+	LGF	R1, V2ADDR	load v2 source
000066AE	E761 0000 0806		00000000	4900+	VL	v22, 0(R1)	use v21 to test decoder
000066B4	E310 5028 0014		00000028	4901+	LGF	R1, V3ADDR	load v3 source
000066BA	E771 0000 0806		00000000	4902+	VL	v23, 0(R1)	use v22 to test decoder
000066C0	E756 7010 2EF9			4903+	VCHL	V21, V22, V23, 2, 1	test instruction
000066C6	B98D 0020			4904+	EPSW	R2, R0	extract psw
000066CA	5020 500C		0000000C	4905+	ST	R2, CCPSW	to save CC
000066CE	E750 5048 080E		00006688	4906+	VST	V21, V10110	save v1 output
000066D4	07FB			4907+	BR	R11	return
000066D8				4908+RE110	DC	0F	V1 for this test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000066D8				4909+	DROP	R5	
000066D8	00000000 00000000			4910	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result t
000066E0	FFFFFFFF 00000000						
000066E8	00000000 00000000			4911	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
000066F0	8FFF8FFF 00000000						
000066F8	00000000 00000000			4912	DC	XL16' 0000000000000000 0000000000000000'	v2
00006700	00000000 00000000						
				4913			
				4914	VRR_B	VCHL, 2, 3	
00006708				4915+	DS	0FD	
00006708		00006708		4916+	USING	*, R5	base for test data and test routine
00006708	00006770			4917+T111	DC	A(X111)	address of test routine
0000670C	006F			4918+	DC	H' 111'	test number
0000670E	00			4919+	DC	X' 00'	
0000670F	02			4920+	DC	HL1' 2'	m4 used
00006710	01			4921+	DC	HL1' 1'	m5 used
00006711	03			4922+	DC	HL1' 3'	CC
00006712	0E			4923+	DC	HL1' 14'	CC failed mask
00006714	00000000 00000000			4924+	DS	2F	extracted PSW after test (has CC)
0000671C	FF			4925+	DC	X' FF'	extracted CC, if test failed
0000671D	E5C3C8D3 40404040			4926+	DC	CL8' VCHL'	instruction name
00006728	000067A0			4927+	DC	A(RE111)	address of v1 result
0000672C	000067B0			4928+	DC	A(RE111+16)	address of v2 source
00006730	000067C0			4929+	DC	A(RE111+32)	address of v3 source
00006734	00000010			4930+	DC	A(16)	result length
00006738	000067A0			4931+REA111	DC	A(RE111)	result address
00006740	00000000 00000000			4932+	DS	2FD	gap
00006748	00000000 00000000						
00006750	00000000 00000000			4933+V10111	DS	XL16	V1 output
00006758	00000000 00000000						
00006760	00000000 00000000			4934+	DS	2FD	gap
00006768	00000000 00000000						
				4935+*			
00006770				4936+X111	DS	0F	
00006770	E310 5024 0014		00000024	4937+	LGF	R1, V2ADDR	load v2 source
00006776	E761 0000 0806		00000000	4938+	VL	v22, 0(R1)	use v21 to test decoder
0000677C	E310 5028 0014		00000028	4939+	LGF	R1, V3ADDR	load v3 source
00006782	E771 0000 0806		00000000	4940+	VL	v23, 0(R1)	use v22 to test decoder
00006788	E756 7010 2EF9			4941+	VCHL	V21, V22, V23, 2, 1	test instruction
0000678E	B98D 0020			4942+	EPSW	R2, R0	extract psw
00006792	5020 500C		0000000C	4943+	ST	R2, CCPSW	to save CC
00006796	E750 5048 080E		00006750	4944+	VST	V21, V10111	save v1 output
0000679C	07FB			4945+	BR	R11	return
000067A0				4946+RE111	DC	0F	V1 for this test
000067A0				4947+	DROP	R5	
000067A0	00000000 00000000			4948	DC	XL16' 0000000000000000 0000000000000000'	result t
000067A8	00000000 00000000						
000067B0	00000000 00000000			4949	DC	XL16' 0000000000000000 0000000000000000'	v2
000067B8	00000000 00000000						
000067C0	00000000 00000000			4950	DC	XL16' 0000000000000000 0000000000000000'	v3
000067C8	00000000 00000000						
				4951			
				4952 *Doubleword			
				4953	VRR_B	VCHL, 3, 0	
000067D0				4954+	DS	0FD	
000067D0		000067D0		4955+	USING	*, R5	base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000067D0	00006838			4956+T112	DC	A(X112) address of test routine
000067D4	0070			4957+	DC	H' 112' test number
000067D6	00			4958+	DC	X' 00'
000067D7	03			4959+	DC	HL1' 3' m4 used
000067D8	01			4960+	DC	HL1' 1' m5 used
000067D9	00			4961+	DC	HL1' 0' CC
000067DA	07			4962+	DC	HL1' 7' CC failed mask
000067DC	00000000 00000000			4963+	DS	2F extracted PSW after test (has CC)
000067E4	FF			4964+	DC	X' FF' extracted CC, if test failed
000067E5	E5C3C8D3 40404040			4965+	DC	CL8' VCHL' instruction name
000067F0	00006868			4966+	DC	A(RE112) address of v1 result
000067F4	00006878			4967+	DC	A(RE112+16) address of v2 source
000067F8	00006888			4968+	DC	A(RE112+32) address of v3 source
000067FC	00000010			4969+	DC	A(16) result length
00006800	00006868			4970+REA112	DC	A(RE112) result address
00006808	00000000 00000000			4971+	DS	2FD gap
00006810	00000000 00000000					
00006818	00000000 00000000			4972+V10112	DS	XL16 V1 output
00006820	00000000 00000000					
00006828	00000000 00000000			4973+	DS	2FD gap
00006830	00000000 00000000					
				4974+*		
00006838				4975+X112	DS	0F
00006838	E310 5024 0014		00000024	4976+	LGF	R1, V2ADDR load v2 source
0000683E	E761 0000 0806		00000000	4977+	VL	v22, 0(R1) use v21 to test decoder
00006844	E310 5028 0014		00000028	4978+	LGF	R1, V3ADDR load v3 source
0000684A	E771 0000 0806		00000000	4979+	VL	v23, 0(R1) use v22 to test decoder
00006850	E756 7010 3EF9			4980+	VCHL	V21, V22, V23, 3, 1 test instruction
00006856	B98D 0020			4981+	EPSW	R2, R0 extract psw
0000685A	5020 500C		0000000C	4982+	ST	R2, CCPSW to save CC
0000685E	E750 5048 080E		00006818	4983+	VST	V21, V10112 save v1 output
00006864	07FB			4984+	BR	R11 return
00006868				4985+RE112	DC	0F V1 for this test
00006868				4986+	DROP	R5
00006868	FFFFFFFF FFFFFFFF			4987	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF' result t
00006870	FFFFFFFF FFFFFFFF					
00006878	FFFFFFFF FFFFFFFF			4988	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF' v2
00006880	FFFFFFFF FFFFFFFF					
00006888	00000000 00000000			4989	DC	XL16' 0000000000000000 0000000000000000' v3
00006890	00000000 00000000					
				4990		
00006898				4991	VRR_B	VCHL, 3, 1
00006898		00006898		4992+	DS	0FD
00006898	00006900			4993+	USING	*, R5 base for test data and test routine
0000689C	0071			4994+T113	DC	A(X113) address of test routine
0000689E	00			4995+	DC	H' 113' test number
0000689F	03			4996+	DC	X' 00'
000068A0	01			4997+	DC	HL1' 3' m4 used
000068A1	01			4998+	DC	HL1' 1' m5 used
000068A2	0B			4999+	DC	HL1' 1' CC
000068A4	00000000 00000000			5000+	DC	HL1' 11' CC failed mask
000068AC	FF			5001+	DS	2F extracted PSW after test (has CC)
000068AD	E5C3C8D3 40404040			5002+	DC	X' FF' extracted CC, if test failed
000068B8	00006930			5003+	DC	CL8' VCHL' instruction name
000068BC	00006940			5004+	DC	A(RE113) address of v1 result
				5005+	DC	A(RE113+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000068C0	00006950			5006+	DC	A(RE113+32)	address of v3 source
000068C4	00000010			5007+	DC	A(16)	result length
000068C8	00006930			5008+REA113	DC	A(RE113)	result address
000068D0	00000000 00000000			5009+	DS	2FD	gap
000068D8	00000000 00000000						
000068E0	00000000 00000000			5010+V10113	DS	XL16	V1 output
000068E8	00000000 00000000						
000068F0	00000000 00000000			5011+	DS	2FD	gap
000068F8	00000000 00000000						
00006900				5012+*			
00006900	E310 5024 0014		00000024	5013+X113	DS	0F	
00006906	E761 0000 0806		00000000	5014+	LGF	R1, V2ADDR	load v2 source
0000690C	E310 5028 0014		00000028	5015+	VL	v22, 0(R1)	use v21 to test decoder
00006912	E771 0000 0806		00000000	5016+	LGF	R1, V3ADDR	load v3 source
00006918	E756 7010 3EF9			5017+	VL	v23, 0(R1)	use v22 to test decoder
0000691E	B98D 0020			5018+	VCHL	V21, V22, V23, 3, 1	test instruction
00006922	5020 500C		0000000C	5019+	EPSW	R2, R0	extract psw
00006926	E750 5048 080E		000068E0	5020+	ST	R2, CCPSW	to save CC
0000692C	07FB			5021+	VST	V21, V10113	save v1 output
00006930				5022+	BR	R11	return
00006930				5023+RE113	DC	0F	V1 for this test
00006930	00000000 00000000			5024+	DROP	R5	
00006930	00000000 00000000			5025	DC	XL16' 0000000000000000 0000000000000000	result t
00006938	FFFFFFFF FFFFFFFF						
00006940	00000000 00000000			5026	DC	XL16' 0000000000000000 8FFF8FFF00000000'	v3
00006948	8FFF8FFF 00000000						
00006950	00000000 00000000			5027	DC	XL16' 0000000000000000 0000000000000000'	v2
00006958	00000000 00000000						
00006960				5028			
00006960		00006960		5029	VRR_B	VCHL, 3, 3	
00006960	000069C8			5030+	DS	0FD	
00006964	0072			5031+	USING	*, R5	base for test data and test routine
00006966	00			5032+T114	DC	A(X114)	address of test routine
00006967	03			5033+	DC	H' 114'	test number
00006968	01			5034+	DC	X' 00'	
00006969	03			5035+	DC	HL1' 3'	m4 used
0000696A	0E			5036+	DC	HL1' 1'	m5 used
0000696C	00000000 00000000			5037+	DC	HL1' 3'	CC
00006974	FF			5038+	DC	HL1' 14'	CC failed mask
00006975	E5C3C8D3 40404040			5039+	DS	2F	extracted PSW after test (has CC)
00006980	000069F8			5040+	DC	X' FF'	extracted CC, if test failed
00006984	00006A08			5041+	DC	CL8' VCHL'	instruction name
00006988	00006A18			5042+	DC	A(RE114)	address of v1 result
0000698C	00000010			5043+	DC	A(RE114+16)	address of v2 source
00006990	000069F8			5044+	DC	A(RE114+32)	address of v3 source
00006998	00000000 00000000			5045+	DC	A(16)	result length
000069A0	00000000 00000000			5046+REA114	DC	A(RE114)	result address
000069A8	00000000 00000000			5047+	DS	2FD	gap
000069B0	00000000 00000000						
000069B8	00000000 00000000			5048+V10114	DS	XL16	V1 output
000069C0	00000000 00000000						
000069C8				5049+	DS	2FD	gap
000069C8	E310 5024 0014		00000024	5050+*			
000069C8				5051+X114	DS	0F	
000069C8				5052+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000069CE	E761 0000 0806		00000000	5053+	VL	v22, 0(R1)	use v21 to test decoder
000069D4	E310 5028 0014		00000028	5054+	LGF	R1, V3ADDR	load v3 source
000069DA	E771 0000 0806		00000000	5055+	VL	v23, 0(R1)	use v22 to test decoder
000069E0	E756 7010 3EF9			5056+	VCHL	V21, V22, V23, 3, 1	test instruction
000069E6	B98D 0020			5057+	EPSW	R2, R0	extract psw
000069EA	5020 500C		0000000C	5058+	ST	R2, CCPSW	to save CC
000069EE	E750 5048 080E		000069A8	5059+	VST	V21, V10114	save v1 output
000069F4	07FB			5060+	BR	R11	return
000069F8				5061+RE114	DC	0F	V1 for this test
000069F8				5062+	DROP	R5	
000069F8	00000000 00000000			5063	DC	XL16' 0000000000000000 0000000000000000'	result t
00006A00	00000000 00000000						
00006A08	00000000 00000000			5064	DC	XL16' 0000000000000000 0000000000000000'	v2
00006A10	00000000 00000000						
00006A18	00000000 00000000			5065	DC	XL16' 0000000000000000 0000000000000000'	v3
00006A20	00000000 00000000						
				5066			
				5067 *			
				5068 * case - general			
				5069 *			
				5070 *Byte			
				5071	VRR_B	VCHL, 0, 0	
00006A28				5072+	DS	0FD	
00006A28		00006A28		5073+	USING	*, R5	base for test data and test routine
00006A28	00006A90			5074+T115	DC	A(X115)	address of test routine
00006A2C	0073			5075+	DC	H' 115'	test number
00006A2E	00			5076+	DC	X' 00'	
00006A2F	00			5077+	DC	HL1' 0'	m4 used
00006A30	01			5078+	DC	HL1' 1'	m5 used
00006A31	00			5079+	DC	HL1' 0'	CC
00006A32	07			5080+	DC	HL1' 7'	CC failed mask
00006A34	00000000 00000000			5081+	DS	2F	extracted PSW after test (has CC)
00006A3C	FF			5082+	DC	X' FF'	extracted CC, if test failed
00006A3D	E5C3C8D3 40404040			5083+	DC	CL8' VCHL'	instruction name
00006A48	00006AC0			5084+	DC	A(RE115)	address of v1 result
00006A4C	00006AD0			5085+	DC	A(RE115+16)	address of v2 source
00006A50	00006AE0			5086+	DC	A(RE115+32)	address of v3 source
00006A54	00000010			5087+	DC	A(16)	result length
00006A58	00006AC0			5088+REA115	DC	A(RE115)	result address
00006A60	00000000 00000000			5089+	DS	2FD	gap
00006A68	00000000 00000000						
00006A70	00000000 00000000			5090+V10115	DS	XL16	V1 output
00006A78	00000000 00000000						
00006A80	00000000 00000000			5091+	DS	2FD	gap
00006A88	00000000 00000000						
				5092+*			
00006A90				5093+X115	DS	0F	
00006A90	E310 5024 0014		00000024	5094+	LGF	R1, V2ADDR	load v2 source
00006A96	E761 0000 0806		00000000	5095+	VL	v22, 0(R1)	use v21 to test decoder
00006A9C	E310 5028 0014		00000028	5096+	LGF	R1, V3ADDR	load v3 source
00006AA2	E771 0000 0806		00000000	5097+	VL	v23, 0(R1)	use v22 to test decoder
00006AA8	E756 7010 0EF9			5098+	VCHL	V21, V22, V23, 0, 1	test instruction
00006AAE	B98D 0020			5099+	EPSW	R2, R0	extract psw
00006AB2	5020 500C		0000000C	5100+	ST	R2, CCPSW	to save CC
00006AB6	E750 5048 080E		00006A70	5101+	VST	V21, V10115	save v1 output
00006ABC	07FB			5102+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006AC0				5103+RE115	DC	0F	V1 for this test
00006AC0				5104+	DROP	R5	
00006AC0	FFFFFFFF FFFFFFFF			5105	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00006AC8	FFFFFFFF FFFFFFFF						
00006AD0	01020304 05060708			5106	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00006AD8	090A0B0C 0D0E0F10						
00006AE0	00010203 04050607			5107	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00006AE8	08090A0B 0C0D0E0F						
				5108			
00006AF0				5109	VRR_B	VCHL, 0, 0	
00006AF0		00006AF0		5110+	DS	0FD	
00006AF0	00006B58			5111+	USING	*, R5	base for test data and test routine
00006AF4	0074			5112+T116	DC	A(X116)	address of test routine
00006AF6	00			5113+	DC	H' 116'	test number
00006AF7	00			5114+	DC	X' 00'	
00006AF8	01			5115+	DC	HL1' 0'	m4 used
00006AF9	00			5116+	DC	HL1' 1'	m5 used
00006AFA	07			5117+	DC	HL1' 0'	CC
00006AFC	00000000 00000000			5118+	DC	HL1' 7'	CC failed mask
00006B04	FF			5119+	DS	2F	extracted PSW after test (has CC)
00006B05	E5C3C8D3 40404040			5120+	DC	X' FF'	extracted CC, if test failed
00006B10	00006B88			5121+	DC	CL8' VCHL'	instruction name
00006B14	00006B98			5122+	DC	A(RE116)	address of v1 result
00006B18	00006BA8			5123+	DC	A(RE116+16)	address of v2 source
00006B1C	00000010			5124+	DC	A(RE116+32)	address of v3 source
00006B20	00006B88			5125+	DC	A(16)	result length
00006B28	00000000 00000000			5126+REA116	DC	A(RE116)	result address
00006B30	00000000 00000000			5127+	DS	2FD	gap
00006B38	00000000 00000000			5128+V10116	DS	XL16	V1 output
00006B40	00000000 00000000						
00006B48	00000000 00000000			5129+	DS	2FD	gap
00006B50	00000000 00000000						
				5130+*			
00006B58				5131+X116	DS	0F	
00006B58	E310 5024 0014		00000024	5132+	LGF	R1, V2ADDR	load v2 source
00006B5E	E761 0000 0806		00000000	5133+	VL	v22, 0(R1)	use v21 to test decoder
00006B64	E310 5028 0014		00000028	5134+	LGF	R1, V3ADDR	load v3 source
00006B6A	E771 0000 0806		00000000	5135+	VL	v23, 0(R1)	use v22 to test decoder
00006B70	E756 7010 0EF9			5136+	VCHL	V21, V22, V23, 0, 1	test instruction
00006B76	B98D 0020			5137+	EPSW	R2, R0	extract psw
00006B7A	5020 500C		0000000C	5138+	ST	R2, CCPSW	to save CC
00006B7E	E750 5048 080E		00006B38	5139+	VST	V21, V10116	save v1 output
00006B84	07FB			5140+	BR	R11	return
00006B88				5141+RE116	DC	0F	V1 for this test
00006B88				5142+	DROP	R5	
00006B88	FFFFFFFF FFFFFFFF			5143	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00006B90	FFFFFFFF FFFFFFFF						
00006B98	FFFEFFFD FFFCFFFB			5144	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00006BA0	FFFAFFF9 FFF8FFF7						
00006BA8	00010203 04050607			5145	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00006BB0	08090A0B 0C0D0E0F						
				5146			
00006BB8				5147	VRR_B	VCHL, 0, 1	
00006BB8		00006BB8		5148+	DS	0FD	
				5149+	USING	*, R5	base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00006BB8	00006C20			5150+T117	DC	A(X117)
00006BBC	0075			5151+	DC	H' 117'
00006BBE	00			5152+	DC	X' 00'
00006BBF	00			5153+	DC	HL1' 0'
00006BC0	01			5154+	DC	HL1' 1'
00006BC1	01			5155+	DC	HL1' 1'
00006BC2	0B			5156+	DC	HL1' 11'
00006BC4	00000000 00000000			5157+	DS	2F
00006BCC	FF			5158+	DC	X' FF'
00006BCD	E5C3C8D3 40404040			5159+	DC	CL8' VCHL'
00006BD8	00006C50			5160+	DC	A(RE117)
00006BDC	00006C60			5161+	DC	A(RE117+16)
00006BE0	00006C70			5162+	DC	A(RE117+32)
00006BE4	00000010			5163+	DC	A(16)
00006BE8	00006C50			5164+REA117	DC	A(RE117)
00006BF0	00000000 00000000			5165+	DS	2FD
00006BF8	00000000 00000000					
00006C00	00000000 00000000			5166+V10117	DS	XL16
00006C08	00000000 00000000					
00006C10	00000000 00000000			5167+	DS	2FD
00006C18	00000000 00000000					
00006C20				5168+*		
00006C20	E310 5024 0014			5169+X117	DS	0F
00006C26	E761 0000 0806		00000024	5170+	LGF	R1, V2ADDR
00006C2C	E310 5028 0014		00000000	5171+	VL	v22, 0(R1)
00006C32	E771 0000 0806		00000028	5172+	LGF	R1, V3ADDR
00006C38	E756 7010 0EF9		00000000	5173+	VL	v23, 0(R1)
00006C3E	B98D 0020			5174+	VCHL	V21, V22, V23, 0, 1
00006C42	5020 500C		0000000C	5175+	EPSW	R2, R0
00006C46	E750 5048 080E		00006C00	5176+	ST	R2, CCPSW
00006C4C	07FB			5177+	VST	V21, V10117
00006C50				5178+	BR	R11
00006C50				5179+RE117	DC	0F
00006C50	00FF00FF 00FF00FF			5180+	DROP	R5
00006C58	00000000 000000FF			5181	DC	XL16' 00FF00FF00FF00FF 00000000000000FF'
00006C60	00110033 00550077			5182	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'
00006C68	08090A0B 0C0DFE1F					v2
00006C70	00010203 04050607			5183	DC	XL16' 0001020304050607 08090A0B0C0DFE0F'
00006C78	08090A0B 0C0DFE0F					v3
00006C80				5184		
00006C80				5185	VRR_B	VCHL, 0, 1
00006C80		00006C80		5186+	DS	0FD
00006C80	00006CE8			5187+	USING	*, R5
00006C84	0076			5188+T118	DC	A(X118)
00006C86	00			5189+	DC	H' 118'
00006C87	00			5190+	DC	X' 00'
00006C88	01			5191+	DC	HL1' 0'
00006C89	01			5192+	DC	HL1' 1'
00006C8A	0B			5193+	DC	HL1' 1'
00006C8C	00000000 00000000			5194+	DC	HL1' 11'
00006C94	FF			5195+	DS	2F
00006C95	E5C3C8D3 40404040			5196+	DC	X' FF'
00006CA0	00006D18			5197+	DC	CL8' VCHL'
00006CA4	00006D28			5198+	DC	A(RE118)
				5199+	DC	A(RE118+16)

address of test routine
test numberm4 used
m5 usedCC
CC failed mask
extracted PSW after test (has CC)
extracted CC, if test failedinstruction name
address of v1 result
address of v2 source
address of v3 source
result length
result address
gap

V1 output

gap

load v2 source
use v21 to test decoder
load v3 source
use v22 to test decoder
test instructionextract psw
to save CC
save v1 output
return
V1 for this test

result t

v2
v3base for test data and test routine
address of test routine
test numberm4 used
m5 usedCC
CC failed mask
extracted PSW after test (has CC)
extracted CC, if test failedinstruction name
address of v1 result
address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006CA8	00006D38			5200+	DC	A(RE118+32)	address of v3 source
00006CAC	00000010			5201+	DC	A(16)	result length
00006CB0	00006D18			5202+REA118	DC	A(RE118)	result address
00006CB8	00000000 00000000			5203+	DS	2FD	gap
00006CC0	00000000 00000000						
00006CC8	00000000 00000000			5204+V10118	DS	XL16	V1 output
00006CD0	00000000 00000000						
00006CD8	00000000 00000000			5205+	DS	2FD	gap
00006CE0	00000000 00000000						
00006CE8				5206+*			
00006CE8	E310 5024 0014		00000024	5207+X118	DS	0F	
00006CEE	E761 0000 0806		00000000	5208+	LGF	R1, V2ADDR	load v2 source
00006CF4	E310 5028 0014		00000028	5209+	VL	v22, 0(R1)	use v21 to test decoder
00006CFA	E771 0000 0806		00000000	5210+	LGF	R1, V3ADDR	load v3 source
00006D00	E756 7010 0EF9			5211+	VL	v23, 0(R1)	use v22 to test decoder
00006D06	B98D 0020			5212+	VCHL	V21, V22, V23, 0, 1	test instruction
00006D0A	5020 500C		0000000C	5213+	EPSW	R2, R0	extract psw
00006D0E	E750 5048 080E		00006CC8	5214+	ST	R2, CCPSW	to save CC
00006D14	07FB			5215+	VST	V21, V10118	save v1 output
00006D18				5216+	BR	R11	return
00006D18				5217+RE118	DC	0F	V1 for this test
00006D18				5218+	DROP	R5	
00006D18	00000000 000000FF			5219	DC	XL16' 00000000000000FF 00FF00FF00FF00FF'	result t
00006D20	00FF00FF 00FF00FF						
00006D28	08090A0B 0C0DFE1F			5220	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
00006D30	00110033 00550077						
00006D38	08090A0B 0C0DFE0F			5221	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v3
00006D40	00010203 04050607						
00006D48				5222			
00006D48				5223	VRR_B	VCHL, 0, 3	
00006D48		00006D48		5224+	DS	0FD	
00006D48	00006DB0			5225+	USING	*, R5	base for test data and test routine
00006D4C	0077			5226+T119	DC	A(X119)	address of test routine
00006D4E	00			5227+	DC	H' 119'	test number
00006D4F	00			5228+	DC	X' 00'	
00006D50	01			5229+	DC	HL1' 0'	m4 used
00006D51	03			5230+	DC	HL1' 1'	m5 used
00006D52	0E			5231+	DC	HL1' 3'	CC
00006D54	00000000 00000000			5232+	DC	HL1' 14'	CC failed mask
00006D5C	FF			5233+	DS	2F	extracted PSW after test (has CC)
00006D5D	E5C3C8D3 40404040			5234+	DC	X' FF'	extracted CC, if test failed
00006D68	00006DE0			5235+	DC	CL8' VCHL'	instruction name
00006D6C	00006DF0			5236+	DC	A(RE119)	address of v1 result
00006D70	00006E00			5237+	DC	A(RE119+16)	address of v2 source
00006D74	00000010			5238+	DC	A(RE119+32)	address of v3 source
00006D78	00006DE0			5239+	DC	A(16)	result length
00006D80	00000000 00000000			5240+REA119	DC	A(RE119)	result address
00006D88	00000000 00000000			5241+	DS	2FD	gap
00006D90	00000000 00000000			5242+V10119	DS	XL16	V1 output
00006D98	00000000 00000000						
00006DA0	00000000 00000000			5243+	DS	2FD	gap
00006DA8	00000000 00000000						
00006DB0				5244+*			
00006DB0	E310 5024 0014		00000024	5245+X119	DS	0F	
00006DB0				5246+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006DB6	E761 0000 0806		00000000	5247+	VL	v22, 0(R1)	use v21 to test decoder
00006DBC	E310 5028 0014		00000028	5248+	LGF	R1, V3ADDR	load v3 source
00006DC2	E771 0000 0806		00000000	5249+	VL	v23, 0(R1)	use v22 to test decoder
00006DC8	E756 7010 0EF9			5250+	VCHL	V21, V22, V23, 0, 1	test instruction
00006DCE	B98D 0020			5251+	EPSW	R2, R0	extract psw
00006DD2	5020 500C		0000000C	5252+	ST	R2, CCPSW	to save CC
00006DD6	E750 5048 080E		00006D90	5253+	VST	V21, V10119	save v1 output
00006DDC	07FB			5254+	BR	R11	return
00006DE0				5255+RE119	DC	0F	V1 for this test
00006DE0				5256+	DROP	R5	
00006DE0	00000000 00000000			5257	DC	XL16' 0000000000000000 0000000000000000'	result t
00006DE8	00000000 00000000						
00006DF0	00010003 04050607			5258	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00006DF8	00090A0B 0C0D0E0F						
00006E00	01110233 11550677			5259	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3
00006E08	119911BB F1DD11FF						
				5260			
00006E10				5261	VRR_B	VCHL, 0, 3	
00006E10		00006E10		5262+	DS	0FD	
00006E10	00006E78			5263+	USING	*, R5	base for test data and test routine
00006E14	0078			5264+T120	DC	A(X120)	address of test routine
00006E16	00			5265+	DC	H' 120'	test number
00006E17	00			5266+	DC	X' 00'	
00006E18	01			5267+	DC	HL1' 0'	m4 used
00006E19	03			5268+	DC	HL1' 1'	m5 used
00006E1A	0E			5269+	DC	HL1' 3'	CC
00006E1C	00000000 00000000			5270+	DC	HL1' 14'	CC failed mask
00006E24	FF			5271+	DS	2F	extracted PSW after test (has CC)
00006E25	E5C3C8D3 40404040			5272+	DC	X' FF'	extracted CC, if test failed
00006E30	00006EA8			5273+	DC	CL8' VCHL'	instruction name
00006E34	00006EB8			5274+	DC	A(RE120)	address of v1 result
00006E38	00006EC8			5275+	DC	A(RE120+16)	address of v2 source
00006E3C	00000010			5276+	DC	A(RE120+32)	address of v3 source
00006E40	00006EA8			5277+	DC	A(16)	result length
00006E48	00000000 00000000			5278+REA120	DC	A(RE120)	result address
00006E50	00000000 00000000			5279+	DS	2FD	gap
00006E58	00000000 00000000			5280+V10120	DS	XL16	V1 output
00006E60	00000000 00000000						
00006E68	00000000 00000000			5281+	DS	2FD	gap
00006E70	00000000 00000000						
				5282+*			
00006E78				5283+X120	DS	0F	
00006E78	E310 5024 0014		00000024	5284+	LGF	R1, V2ADDR	load v2 source
00006E7E	E761 0000 0806		00000000	5285+	VL	v22, 0(R1)	use v21 to test decoder
00006E84	E310 5028 0014		00000028	5286+	LGF	R1, V3ADDR	load v3 source
00006E8A	E771 0000 0806		00000000	5287+	VL	v23, 0(R1)	use v22 to test decoder
00006E90	E756 7010 0EF9			5288+	VCHL	V21, V22, V23, 0, 1	test instruction
00006E96	B98D 0020			5289+	EPSW	R2, R0	extract psw
00006E9A	5020 500C		0000000C	5290+	ST	R2, CCPSW	to save CC
00006E9E	E750 5048 080E		00006E58	5291+	VST	V21, V10120	save v1 output
00006EA4	07FB			5292+	BR	R11	return
00006EA8				5293+RE120	DC	0F	V1 for this test
00006EA8				5294+	DROP	R5	
00006EA8	00000000 00000000			5295	DC	XL16' 0000000000000000 0000000000000000'	result t
00006EB0	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00006EB8	08090A0B 0C0D0E0F			5296	DC	XL16' 08090A0B0C0D0E0F	0001020304050607'	v2
00006EC0	00010203 04050607							
00006EC8	119911BB F1DD11FF			5297	DC	XL16' 119911BBF1DD11FF	0111023311550677'	v3
00006ED0	01110233 11550677							
				5298				
				5299	*Halfword			
				5300	VRR_B	VCHL, 1, 0		
00006ED8				5301+	DS	0FD		
00006ED8		00006ED8		5302+	USING	*, R5	base for test data and test routine	
00006ED8	00006F40			5303+T121	DC	A(X121)	address of test routine	
00006EDC	0079			5304+	DC	H' 121'	test number	
00006EDE	00			5305+	DC	X' 00'		
00006EDF	01			5306+	DC	HL1' 1'	m4 used	
00006EE0	01			5307+	DC	HL1' 1'	m5 used	
00006EE1	00			5308+	DC	HL1' 0'	CC	
00006EE2	07			5309+	DC	HL1' 7'	CC failed mask	
00006EE4	00000000 00000000			5310+	DS	2F	extracted PSW after test (has CC)	
00006EEC	FF			5311+	DC	X' FF'	extracted CC, if test failed	
00006EED	E5C3C8D3 40404040			5312+	DC	CL8' VCHL'	instruction name	
00006EF8	00006F70			5313+	DC	A(RE121)	address of v1 result	
00006EFC	00006F80			5314+	DC	A(RE121+16)	address of v2 source	
00006F00	00006F90			5315+	DC	A(RE121+32)	address of v3 source	
00006F04	00000010			5316+	DC	A(16)	result length	
00006F08	00006F70			5317+REA121	DC	A(RE121)	result address	
00006F10	00000000 00000000			5318+	DS	2FD	gap	
00006F18	00000000 00000000							
00006F20	00000000 00000000			5319+V10121	DS	XL16	V1 output	
00006F28	00000000 00000000							
00006F30	00000000 00000000			5320+	DS	2FD	gap	
00006F38	00000000 00000000							
				5321+*				
00006F40				5322+X121	DS	0F		
00006F40	E310 5024 0014		00000024	5323+	LGF	R1, V2ADDR	load v2 source	
00006F46	E761 0000 0806		00000000	5324+	VL	v22, 0(R1)	use v21 to test decoder	
00006F4C	E310 5028 0014		00000028	5325+	LGF	R1, V3ADDR	load v3 source	
00006F52	E771 0000 0806		00000000	5326+	VL	v23, 0(R1)	use v22 to test decoder	
00006F58	E756 7010 1EF9			5327+	VCHL	V21, V22, V23, 1, 1	test instruction	
00006F5E	B98D 0020			5328+	EPSW	R2, R0	extract psw	
00006F62	5020 500C		0000000C	5329+	ST	R2, CCPSW	to save CC	
00006F66	E750 5048 080E		00006F20	5330+	VST	V21, V10121	save v1 output	
00006F6C	07FB			5331+	BR	R11	return	
00006F70				5332+RE121	DC	0F	V1 for this test	
00006F70				5333+	DROP	R5		
00006F70	FFFFFFFF FFFFFFFF			5334	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00006F78	FFFFFFFF FFFFFFFF							
00006F80	01020304 05060708			5335	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2	
00006F88	090A0B0C 0D0E0F10							
00006F90	00010203 04050607			5336	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3	
00006F98	08090A0B 0C0D0E0F							
				5337				
				5338	VRR_B	VCHL, 1, 0		
00006FA0				5339+	DS	0FD		
00006FA0		00006FA0		5340+	USING	*, R5	base for test data and test routine	
00006FA0	00007008			5341+T122	DC	A(X122)	address of test routine	
00006FA4	007A			5342+	DC	H' 122'	test number	
00006FA6	00			5343+	DC	X' 00'		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00006FA7	01			5344+	DC	HL1' 1' m4 used
00006FA8	01			5345+	DC	HL1' 1' m5 used
00006FA9	00			5346+	DC	HL1' 0' CC
00006FAA	07			5347+	DC	HL1' 7' CC failed mask
00006FAC	00000000	00000000		5348+	DS	2F extracted PSW after test (has CC)
00006FB4	FF			5349+	DC	X' FF' extracted CC, if test failed
00006FB5	E5C3C8D3	40404040		5350+	DC	CL8' VCHL' instruction name
00006FC0	00007038			5351+	DC	A(RE122) address of v1 result
00006FC4	00007048			5352+	DC	A(RE122+16) address of v2 source
00006FC8	00007058			5353+	DC	A(RE122+32) address of v3 source
00006FCC	00000010			5354+	DC	A(16) result length
00006FD0	00007038			5355+REA122	DC	A(RE122) result address
00006FD8	00000000	00000000		5356+	DS	2FD gap
00006FE0	00000000	00000000				
00006FE8	00000000	00000000		5357+V10122	DS	XL16 V1 output
00006FF0	00000000	00000000				
00006FF8	00000000	00000000		5358+	DS	2FD gap
00007000	00000000	00000000				
				5359+*		
00007008				5360+X122	DS	0F
00007008	E310 5024 0014		00000024	5361+	LGF	R1, V2ADDR load v2 source
0000700E	E761 0000 0806		00000000	5362+	VL	v22, 0(R1) use v21 to test decoder
00007014	E310 5028 0014		00000028	5363+	LGF	R1, V3ADDR load v3 source
0000701A	E771 0000 0806		00000000	5364+	VL	v23, 0(R1) use v22 to test decoder
00007020	E756 7010 1EF9			5365+	VCHL	V21, V22, V23, 1, 1 test instruction
00007026	B98D 0020			5366+	EPSW	R2, R0 extract psw
0000702A	5020 500C		0000000C	5367+	ST	R2, CCPSW to save CC
0000702E	E750 5048 080E		00006FE8	5368+	VST	V21, V10122 save v1 output
00007034	07FB			5369+	BR	R11 return
00007038				5370+RE122	DC	0F V1 for this test
00007038				5371+	DROP	R5
00007038	FFFFFFFF FFFFFFFF			5372	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF' result t
00007040	FFFFFFFF FFFFFFFF					
00007048	FFFEFFFD FFFCFFFB			5373	DC	XL16' FFFEFFFDFFFCFFFB FFFAFF9FFF8FFF7' v2
00007050	FFFAFFF9 FFF8FFF7					
00007058	00010203 04050607			5374	DC	XL16' 0001020304050607 08090A0B0C0D0E0F' v3
00007060	08090A0B 0C0D0E0F					
				5375		
				5376	VRR_B	VCHL, 1, 1
00007068				5377+	DS	0FD
00007068		00007068		5378+	USING	*, R5 base for test data and test routine
00007068	000070D0			5379+T123	DC	A(X123) address of test routine
0000706C	007B			5380+	DC	H' 123' test number
0000706E	00			5381+	DC	X' 00'
0000706F	01			5382+	DC	HL1' 1' m4 used
00007070	01			5383+	DC	HL1' 1' m5 used
00007071	01			5384+	DC	HL1' 1' CC
00007072	0B			5385+	DC	HL1' 11' CC failed mask
00007074	00000000	00000000		5386+	DS	2F extracted PSW after test (has CC)
0000707C	FF			5387+	DC	X' FF' extracted CC, if test failed
0000707D	E5C3C8D3	40404040		5388+	DC	CL8' VCHL' instruction name
00007088	00007100			5389+	DC	A(RE123) address of v1 result
0000708C	00007110			5390+	DC	A(RE123+16) address of v2 source
00007090	00007120			5391+	DC	A(RE123+32) address of v3 source
00007094	00000010			5392+	DC	A(16) result length
00007098	00007100			5393+REA123	DC	A(RE123) result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000070A0	00000000 00000000			5394+	DS	2FD	gap
000070A8	00000000 00000000						
000070B0	00000000 00000000			5395+V10123	DS	XL16	V1 output
000070B8	00000000 00000000						
000070C0	00000000 00000000			5396+	DS	2FD	gap
000070C8	00000000 00000000						
				5397+*			
000070D0				5398+X123	DS	0F	
000070D0	E310 5024 0014		00000024	5399+	LGF	R1, V2ADDR	load v2 source
000070D6	E761 0000 0806		00000000	5400+	VL	v22, 0(R1)	use v21 to test decoder
000070DC	E310 5028 0014		00000028	5401+	LGF	R1, V3ADDR	load v3 source
000070E2	E771 0000 0806		00000000	5402+	VL	v23, 0(R1)	use v22 to test decoder
000070E8	E756 7010 1EF9			5403+	VCHL	V21, V22, V23, 1, 1	test instruction
000070EE	B98D 0020			5404+	EPSW	R2, R0	extract psw
000070F2	5020 500C		0000000C	5405+	ST	R2, CCPSW	to save CC
000070F6	E750 5048 080E		000070B0	5406+	VST	V21, V10123	save v1 output
000070FC	07FB			5407+	BR	R11	return
00007100				5408+RE123	DC	0F	V1 for this test
00007100				5409+	DROP	R5	
00007100	FFFFFFFF FFFFFFFF			5410	DC	XL16' FFFFFFFFFFFFFFFFFF 000000000000FFFF'	result t
00007108	00000000 0000FFFF						
00007110	00110033 00550077			5411	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2
00007118	08090A0B 0C0DFE1F						
00007120	00010023 00450067			5412	DC	XL16' 0001002300450067 08090A0B0C0DFE0F'	v3
00007128	08090A0B 0C0DFE0F						
				5413			
				5414	VRR_B	VCHL, 1, 1	
00007130				5415+	DS	0FD	
00007130		00007130		5416+	USING	*, R5	base for test data and test routine
00007130	00007198			5417+T124	DC	A(X124)	address of test routine
00007134	007C			5418+	DC	H' 124'	test number
00007136	00			5419+	DC	X' 00'	
00007137	01			5420+	DC	HL1' 1'	m4 used
00007138	01			5421+	DC	HL1' 1'	m5 used
00007139	01			5422+	DC	HL1' 1'	CC
0000713A	0B			5423+	DC	HL1' 11'	CC failed mask
0000713C	00000000 00000000			5424+	DS	2F	extracted PSW after test (has CC)
00007144	FF			5425+	DC	X' FF'	extracted CC, if test failed
00007145	E5C3C8D3 40404040			5426+	DC	CL8' VCHL'	instruction name
00007150	000071C8			5427+	DC	A(RE124)	address of v1 result
00007154	000071D8			5428+	DC	A(RE124+16)	address of v2 source
00007158	000071E8			5429+	DC	A(RE124+32)	address of v3 source
0000715C	00000010			5430+	DC	A(16)	result length
00007160	000071C8			5431+REA124	DC	A(RE124)	result address
00007168	00000000 00000000			5432+	DS	2FD	gap
00007170	00000000 00000000						
00007178	00000000 00000000			5433+V10124	DS	XL16	V1 output
00007180	00000000 00000000						
00007188	00000000 00000000			5434+	DS	2FD	gap
00007190	00000000 00000000						
				5435+*			
00007198				5436+X124	DS	0F	
00007198	E310 5024 0014		00000024	5437+	LGF	R1, V2ADDR	load v2 source
0000719E	E761 0000 0806		00000000	5438+	VL	v22, 0(R1)	use v21 to test decoder
000071A4	E310 5028 0014		00000028	5439+	LGF	R1, V3ADDR	load v3 source
000071AA	E771 0000 0806		00000000	5440+	VL	v23, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000071B0	E756 7010 1EF9			5441+	VCHL	V21, V22, V23, 1, 1	test instruction
000071B6	B98D 0020			5442+	EPSW	R2, R0	extract psw
000071BA	5020 500C		0000000C	5443+	ST	R2, CCPSW	to save CC
000071BE	E750 5048 080E		00007178	5444+	VST	V21, V10124	save v1 output
000071C4	07FB			5445+	BR	R11	return
000071C8				5446+RE124	DC	0F	V1 for this test
000071C8				5447+	DROP	R5	
000071C8	00000000 0000FFFF			5448	DC	XL16' 0000000000000000FFFF FFFFFFFFFFFFFFFFFF'	result t
000071D0	FFFFFFFF FFFFFFFF						
000071D8	08090A0B 0C0DFE1F			5449	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
000071E0	00110033 00550077						
000071E8	08090A0B 0C0DFE0F			5450	DC	XL16' 08090A0B0C0DFE0F 0001002300450067'	v3
000071F0	00010023 00450067						
				5451			
				5452	VRR_B	VCHL, 1, 3	
000071F8				5453+	DS	0FD	
000071F8		000071F8		5454+	USING	*, R5	base for test data and test routine
000071F8	00007260			5455+T125	DC	A(X125)	address of test routine
000071FC	007D			5456+	DC	H' 125'	test number
000071FE	00			5457+	DC	X' 00'	
000071FF	01			5458+	DC	HL1' 1'	m4 used
00007200	01			5459+	DC	HL1' 1'	m5 used
00007201	03			5460+	DC	HL1' 3'	CC
00007202	0E			5461+	DC	HL1' 14'	CC failed mask
00007204	00000000 00000000			5462+	DS	2F	extracted PSW after test (has CC)
0000720C	FF			5463+	DC	X' FF'	extracted CC, if test failed
0000720D	E5C3C8D3 40404040			5464+	DC	CL8' VCHL'	instruction name
00007218	00007290			5465+	DC	A(RE125)	address of v1 result
0000721C	000072A0			5466+	DC	A(RE125+16)	address of v2 source
00007220	000072B0			5467+	DC	A(RE125+32)	address of v3 source
00007224	00000010			5468+	DC	A(16)	result length
00007228	00007290			5469+REA125	DC	A(RE125)	result address
00007230	00000000 00000000			5470+	DS	2FD	gap
00007238	00000000 00000000						
00007240	00000000 00000000			5471+V10125	DS	XL16	V1 output
00007248	00000000 00000000						
00007250	00000000 00000000			5472+	DS	2FD	gap
00007258	00000000 00000000						
				5473+*			
00007260				5474+X125	DS	0F	
00007260	E310 5024 0014		00000024	5475+	LGF	R1, V2ADDR	load v2 source
00007266	E761 0000 0806		00000000	5476+	VL	v22, 0(R1)	use v21 to test decoder
0000726C	E310 5028 0014		00000028	5477+	LGF	R1, V3ADDR	load v3 source
00007272	E771 0000 0806		00000000	5478+	VL	v23, 0(R1)	use v22 to test decoder
00007278	E756 7010 1EF9			5479+	VCHL	V21, V22, V23, 1, 1	test instruction
0000727E	B98D 0020			5480+	EPSW	R2, R0	extract psw
00007282	5020 500C		0000000C	5481+	ST	R2, CCPSW	to save CC
00007286	E750 5048 080E		00007240	5482+	VST	V21, V10125	save v1 output
0000728C	07FB			5483+	BR	R11	return
00007290				5484+RE125	DC	0F	V1 for this test
00007290				5485+	DROP	R5	
00007290	00000000 00000000			5486	DC	XL16' 0000000000000000 0000000000000000'	result t
00007298	00000000 00000000						
000072A0	00010003 04050607			5487	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
000072A8	00090A0B 0C0D0E0F						
000072B0	01110233 11550677			5488	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000072B8	119911BB F1DD11FF			5489				
				5490	VRR_B	VCHL, 1, 3		
000072C0				5491+	DS	0FD		
000072C0		000072C0		5492+	USING	*, R5	base for test data and test routine	
000072C0	00007328			5493+T126	DC	A(X126)	address of test routine	
000072C4	007E			5494+	DC	H' 126'	test number	
000072C6	00			5495+	DC	X' 00'		
000072C7	01			5496+	DC	HL1' 1'	m4 used	
000072C8	01			5497+	DC	HL1' 1'	m5 used	
000072C9	03			5498+	DC	HL1' 3'	CC	
000072CA	0E			5499+	DC	HL1' 14'	CC failed mask	
000072CC	00000000 00000000			5500+	DS	2F	extracted PSW after test (has CC)	
000072D4	FF			5501+	DC	X' FF'	extracted CC, if test failed	
000072D5	E5C3C8D3 40404040			5502+	DC	CL8' VCHL'	instruction name	
000072E0	00007358			5503+	DC	A(RE126)	address of v1 result	
000072E4	00007368			5504+	DC	A(RE126+16)	address of v2 source	
000072E8	00007378			5505+	DC	A(RE126+32)	address of v3 source	
000072EC	00000010			5506+	DC	A(16)	result length	
000072F0	00007358			5507+REA126	DC	A(RE126)	result address	
000072F8	00000000 00000000			5508+	DS	2FD	gap	
00007300	00000000 00000000							
00007308	00000000 00000000			5509+V10126	DS	XL16	V1 output	
00007310	00000000 00000000							
00007318	00000000 00000000			5510+	DS	2FD	gap	
00007320	00000000 00000000							
				5511+*				
00007328				5512+X126	DS	0F		
00007328	E310 5024 0014		00000024	5513+	LGF	R1, V2ADDR	load v2 source	
0000732E	E761 0000 0806		00000000	5514+	VL	v22, 0(R1)	use v21 to test decoder	
00007334	E310 5028 0014		00000028	5515+	LGF	R1, V3ADDR	load v3 source	
0000733A	E771 0000 0806		00000000	5516+	VL	v23, 0(R1)	use v22 to test decoder	
00007340	E756 7010 1EF9			5517+	VCHL	V21, V22, V23, 1, 1	test instruction	
00007346	B98D 0020			5518+	EPSW	R2, R0	extract psw	
0000734A	5020 500C		0000000C	5519+	ST	R2, CCPSW	to save CC	
0000734E	E750 5048 080E		00007308	5520+	VST	V21, V10126	save v1 output	
00007354	07FB			5521+	BR	R11	return	
00007358				5522+RE126	DC	0F	V1 for this test	
00007358				5523+	DROP	R5		
00007358	00000000 00000000			5524	DC	XL16' 0000000000000000 0000000000000000'	result t	
00007360	00000000 00000000							
00007368	08090A0B 0C0D0E0F			5525	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2	
00007370	00010203 04050607							
00007378	119911BB F1DD11FF			5526	DC	XL16' 119911BBF1DD11FF 0111023311550677'	v3	
00007380	01110233 11550677							
				5527				
				5528 *Word				
				5529	VRR_B	VCHL, 2, 0		
00007388				5530+	DS	0FD		
00007388		00007388		5531+	USING	*, R5	base for test data and test routine	
00007388	000073F0			5532+T127	DC	A(X127)	address of test routine	
0000738C	007F			5533+	DC	H' 127'	test number	
0000738E	00			5534+	DC	X' 00'		
0000738F	02			5535+	DC	HL1' 2'	m4 used	
00007390	01			5536+	DC	HL1' 1'	m5 used	
00007391	00			5537+	DC	HL1' 0'	CC	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00007392	07			5538+	DC	HL1' 7'
00007394	00000000 00000000			5539+	DS	2F
0000739C	FF			5540+	DC	X' FF'
0000739D	E5C3C8D3 40404040			5541+	DC	CL8' VCHL'
000073A8	00007420			5542+	DC	A(RE127)
000073AC	00007430			5543+	DC	A(RE127+16)
000073B0	00007440			5544+	DC	A(RE127+32)
000073B4	00000010			5545+	DC	A(16)
000073B8	00007420			5546+REA127	DC	A(RE127)
000073C0	00000000 00000000			5547+	DS	2FD
000073C8	00000000 00000000					gap
000073D0	00000000 00000000			5548+V10127	DS	XL16
000073D8	00000000 00000000					V1 output
000073E0	00000000 00000000			5549+	DS	2FD
000073E8	00000000 00000000					gap
000073F0				5550+*		
000073F0	E310 5024 0014		00000024	5551+X127	DS	0F
000073F6	E761 0000 0806		00000000	5552+	LGF	R1, V2ADDR
000073FC	E310 5028 0014		00000028	5553+	VL	v22, 0(R1)
00007402	E771 0000 0806		00000000	5554+	LGF	R1, V3ADDR
00007408	E756 7010 2EF9			5555+	VL	v23, 0(R1)
0000740E	B98D 0020			5556+	VCHL	V21, V22, V23, 2, 1
00007412	5020 500C		0000000C	5557+	EPSW	R2, R0
00007416	E750 5048 080E		000073D0	5558+	ST	R2, CCPSW
0000741C	07FB			5559+	VST	V21, V10127
00007420				5560+	BR	R11
00007420				5561+RE127	DC	0F
00007420				5562+	DROP	R5
00007420	FFFFFFFF FFFFFFFF			5563	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'
00007428	FFFFFFFF FFFFFFFF					result t
00007430	01020304 05060708			5564	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'
00007438	090A0B0C 0D0E0F10					v2
00007440	00010203 04050607			5565	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'
00007448	08090A0B 0C0D0E0F					v3
00007450				5566		
00007450		00007450		5567	VRR_B	VCHL, 2, 0
00007450	000074B8			5568+	DS	0FD
00007454	0080			5569+	USING	*, R5
00007456	00			5570+T128	DC	A(X128)
00007457	02			5571+	DC	H' 128'
00007458	01			5572+	DC	X' 00'
00007459	00			5573+	DC	HL1' 2'
0000745A	07			5574+	DC	HL1' 1'
0000745C	00000000 00000000			5575+	DC	HL1' 0'
00007464	FF			5576+	DC	HL1' 7'
00007465	E5C3C8D3 40404040			5577+	DS	2F
00007470	000074E8			5578+	DC	X' FF'
00007474	000074F8			5579+	DC	CL8' VCHL'
00007478	00007508			5580+	DC	A(RE128)
0000747C	00000010			5581+	DC	A(RE128+16)
00007480	000074E8			5582+	DC	A(RE128+32)
00007488	00000000 00000000			5583+	DC	A(16)
00007490	00000000 00000000			5584+REA128	DC	A(RE128)
00007498	00000000 00000000			5585+	DS	2FD
				5586+V10128	DS	XL16
						V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000074A0	00000000 00000000						
000074A8	00000000 00000000			5587+	DS	2FD	gap
000074B0	00000000 00000000						
				5588+*			
000074B8				5589+X128	DS	0F	
000074B8	E310 5024 0014		00000024	5590+	LGF	R1, V2ADDR	load v2 source
000074BE	E761 0000 0806		00000000	5591+	VL	v22, 0(R1)	use v21 to test decoder
000074C4	E310 5028 0014		00000028	5592+	LGF	R1, V3ADDR	load v3 source
000074CA	E771 0000 0806		00000000	5593+	VL	v23, 0(R1)	use v22 to test decoder
000074D0	E756 7010 2EF9			5594+	VCHL	V21, V22, V23, 2, 1	test instruction
000074D6	B98D 0020			5595+	EPSW	R2, R0	extract psw
000074DA	5020 500C		0000000C	5596+	ST	R2, CCPSW	to save CC
000074DE	E750 5048 080E		00007498	5597+	VST	V21, V10128	save v1 output
000074E4	07FB			5598+	BR	R11	return
000074E8				5599+RE128	DC	0F	V1 for this test
000074E8				5600+	DROP	R5	
000074E8	FFFFFFFF FFFFFFFF			5601	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000074F0	FFFFFFFF FFFFFFFF						
000074F8	FFFEFFFD FFFCFFFB			5602	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
00007500	FFFAFFF9 FFF8FFF7						
00007508	00010203 04050607			5603	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00007510	08090A0B 0C0D0E0F						
				5604			
00007518				5605	VRR_B	VCHL, 2, 1	
00007518		00007518		5606+	DS	0FD	
00007518	00007580			5607+	USING	*, R5	base for test data and test routine
0000751C	0081			5608+T129	DC	A(X129)	address of test routine
0000751E	00			5609+	DC	H' 129'	test number
0000751E	00			5610+	DC	X' 00'	
0000751F	02			5611+	DC	HL1' 2'	m4 used
00007520	01			5612+	DC	HL1' 1'	m5 used
00007521	01			5613+	DC	HL1' 1'	CC
00007522	0B			5614+	DC	HL1' 11'	CC failed mask
00007524	00000000 00000000			5615+	DS	2F	extracted PSW after test (has CC)
0000752C	FF			5616+	DC	X' FF'	extracted CC, if test failed
0000752D	E5C3C8D3 40404040			5617+	DC	CL8' VCHL'	instruction name
00007538	000075B0			5618+	DC	A(RE129)	address of v1 result
0000753C	000075C0			5619+	DC	A(RE129+16)	address of v2 source
00007540	000075D0			5620+	DC	A(RE129+32)	address of v3 source
00007544	00000010			5621+	DC	A(16)	result length
00007548	000075B0			5622+REA129	DC	A(RE129)	result address
00007550	00000000 00000000			5623+	DS	2FD	gap
00007558	00000000 00000000						
00007560	00000000 00000000			5624+V10129	DS	XL16	V1 output
00007568	00000000 00000000						
00007570	00000000 00000000			5625+	DS	2FD	gap
00007578	00000000 00000000						
				5626+*			
00007580				5627+X129	DS	0F	
00007580	E310 5024 0014		00000024	5628+	LGF	R1, V2ADDR	load v2 source
00007586	E761 0000 0806		00000000	5629+	VL	v22, 0(R1)	use v21 to test decoder
0000758C	E310 5028 0014		00000028	5630+	LGF	R1, V3ADDR	load v3 source
00007592	E771 0000 0806		00000000	5631+	VL	v23, 0(R1)	use v22 to test decoder
00007598	E756 7010 2EF9			5632+	VCHL	V21, V22, V23, 2, 1	test instruction
0000759E	B98D 0020			5633+	EPSW	R2, R0	extract psw
000075A2	5020 500C		0000000C	5634+	ST	R2, CCPSW	to save CC

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000075A6	E750 5048 080E		00007560	5635+	VST	V21, V10129	save v1 output	
000075AC	07FB			5636+	BR	R11	return	
000075B0				5637+RE129	DC	0F	V1 for this test	
000075B0				5638+	DROP	R5		
000075B0	FFFFFFFF FFFFFFFF			5639	DC	XL16' FFFFFFFFFFFFFFFFFF 00000000FFFFFFFF'	result t	
000075B8	00000000 FFFFFFFF							
000075C0	00110033 00550077			5640	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2	
000075C8	08090A0B 0C0DFE1F							
000075D0	00010023 00450067			5641	DC	XL16' 0001002300450067 08090A0B0C0DFE0F'	v3	
000075D8	08090A0B 0C0DFE0F							
				5642				
000075E0				5643	VRR_B	VCHL, 2, 1		
000075E0		000075E0		5644+	DS	0FD		
000075E0	00007648			5645+	USING	*, R5	base for test data and test routine	
000075E4	0082			5646+T130	DC	A(X130)	address of test routine	
000075E6	00			5647+	DC	H' 130'	test number	
000075E7	02			5648+	DC	X' 00'		
000075E7	02			5649+	DC	HL1' 2'	m4 used	
000075E8	01			5650+	DC	HL1' 1'	m5 used	
000075E9	01			5651+	DC	HL1' 1'	CC	
000075EA	0B			5652+	DC	HL1' 11'	CC failed mask	
000075EC	00000000 00000000			5653+	DS	2F	extracted PSW after test (has CC)	
000075F4	FF			5654+	DC	X' FF'	extracted CC, if test failed	
000075F5	E5C3C8D3 40404040			5655+	DC	CL8' VCHL'	instruction name	
00007600	00007678			5656+	DC	A(RE130)	address of v1 result	
00007604	00007688			5657+	DC	A(RE130+16)	address of v2 source	
00007608	00007698			5658+	DC	A(RE130+32)	address of v3 source	
0000760C	00000010			5659+	DC	A(16)	result length	
00007610	00007678			5660+REA130	DC	A(RE130)	result address	
00007618	00000000 00000000			5661+	DS	2FD	gap	
00007620	00000000 00000000							
00007628	00000000 00000000			5662+V10130	DS	XL16	V1 output	
00007630	00000000 00000000							
00007638	00000000 00000000			5663+	DS	2FD	gap	
00007640	00000000 00000000							
				5664+*				
00007648				5665+X130	DS	0F		
00007648	E310 5024 0014		00000024	5666+	LGF	R1, V2ADDR	load v2 source	
0000764E	E761 0000 0806		00000000	5667+	VL	v22, 0(R1)	use v21 to test decoder	
00007654	E310 5028 0014		00000028	5668+	LGF	R1, V3ADDR	load v3 source	
0000765A	E771 0000 0806		00000000	5669+	VL	v23, 0(R1)	use v22 to test decoder	
00007660	E756 7010 2EF9			5670+	VCHL	V21, V22, V23, 2, 1	test instruction	
00007666	B98D 0020			5671+	EPSW	R2, R0	extract psw	
0000766A	5020 500C		0000000C	5672+	ST	R2, CCPSW	to save CC	
0000766E	E750 5048 080E		00007628	5673+	VST	V21, V10130	save v1 output	
00007674	07FB			5674+	BR	R11	return	
00007678				5675+RE130	DC	0F	V1 for this test	
00007678				5676+	DROP	R5		
00007678	00000000 FFFFFFFF			5677	DC	XL16' 00000000FFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00007680	FFFFFFFF FFFFFFFF							
00007688	08090A0B 0C0DFE1F			5678	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2	
00007690	00110033 00550077							
00007698	08090A0B 0C0DFE0F			5679	DC	XL16' 08090A0B0C0DFE0F 0001002300450067'	v3	
000076A0	00010023 00450067							
				5680				
				5681	VRR_B	VCHL, 2, 3		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000076A8				5682+	DS	0FD	
000076A8		000076A8		5683+	USING	*, R5	base for test data and test routine
000076A8	00007710			5684+T131	DC	A(X131)	address of test routine
000076AC	0083			5685+	DC	H' 131'	test number
000076AE	00			5686+	DC	X' 00'	
000076AF	02			5687+	DC	HL1' 2'	m4 used
000076B0	01			5688+	DC	HL1' 1'	m5 used
000076B1	03			5689+	DC	HL1' 3'	CC
000076B2	0E			5690+	DC	HL1' 14'	CC failed mask
000076B4	00000000 00000000			5691+	DS	2F	extracted PSW after test (has CC)
000076BC	FF			5692+	DC	X' FF'	extracted CC, if test failed
000076BD	E5C3C8D3 40404040			5693+	DC	CL8' VCHL'	instruction name
000076C8	00007740			5694+	DC	A(RE131)	address of v1 result
000076CC	00007750			5695+	DC	A(RE131+16)	address of v2 source
000076D0	00007760			5696+	DC	A(RE131+32)	address of v3 source
000076D4	00000010			5697+	DC	A(16)	result length
000076D8	00007740			5698+REA131	DC	A(RE131)	result address
000076E0	00000000 00000000			5699+	DS	2FD	gap
000076E8	00000000 00000000						
000076F0	00000000 00000000			5700+V10131	DS	XL16	V1 output
000076F8	00000000 00000000						
00007700	00000000 00000000			5701+	DS	2FD	gap
00007708	00000000 00000000						
00007710				5702+*			
00007710	E310 5024 0014			5703+X131	DS	0F	
00007716	E761 0000 0806		00000024	5704+	LGF	R1, V2ADDR	load v2 source
0000771C	E310 5028 0014		00000000	5705+	VL	v22, 0(R1)	use v21 to test decoder
00007722	E771 0000 0806		00000028	5706+	LGF	R1, V3ADDR	load v3 source
00007728	E756 7010 2EF9		00000000	5707+	VL	v23, 0(R1)	use v22 to test decoder
0000772E	B98D 0020			5708+	VCHL	V21, V22, V23, 2, 1	test instruction
00007732	5020 500C			5709+	EPSW	R2, R0	extract psw
00007736	E750 5048 080E		0000000C	5710+	ST	R2, CCPSW	to save CC
0000773C	07FB		000076F0	5711+	VST	V21, V10131	save v1 output
00007740				5712+	BR	R11	return
00007740				5713+RE131	DC	0F	V1 for this test
00007740				5714+	DROP	R5	
00007740	00000000 00000000			5715	DC	XL16' 0000000000000000 0000000000000000'	result
00007748	00000000 00000000						
00007750	00010003 04050607			5716	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00007758	00090A0B 0C0D0E0F						
00007760	01110233 11550677			5717	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3
00007768	119911BB F1DD11FF						
00007770				5718			
00007770				5719	VRR_B	VCHL, 2, 3	
00007770		00007770		5720+	DS	0FD	
00007770	000077D8			5721+	USING	*, R5	base for test data and test routine
00007774	0084			5722+T132	DC	A(X132)	address of test routine
00007776	00			5723+	DC	H' 132'	test number
00007777	02			5724+	DC	X' 00'	
00007778	01			5725+	DC	HL1' 2'	m4 used
00007779	03			5726+	DC	HL1' 1'	m5 used
0000777A	0E			5727+	DC	HL1' 3'	CC
0000777C	00000000 00000000			5728+	DC	HL1' 14'	CC failed mask
0000777C	00000000 00000000			5729+	DS	2F	extracted PSW after test (has CC)
00007784	FF			5730+	DC	X' FF'	extracted CC, if test failed
00007785	E5C3C8D3 40404040			5731+	DC	CL8' VCHL'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007790	00007808			5732+	DC	A(RE132)	address of v1 result
00007794	00007818			5733+	DC	A(RE132+16)	address of v2 source
00007798	00007828			5734+	DC	A(RE132+32)	address of v3 source
0000779C	00000010			5735+	DC	A(16)	result length
000077A0	00007808			5736+REA132	DC	A(RE132)	result address
000077A8	00000000 00000000			5737+	DS	2FD	gap
000077B0	00000000 00000000						
000077B8	00000000 00000000			5738+V10132	DS	XL16	V1 output
000077C0	00000000 00000000						
000077C8	00000000 00000000			5739+	DS	2FD	gap
000077D0	00000000 00000000						
000077D8				5740+*			
000077D8	E310 5024 0014		00000024	5741+X132	DS	0F	
000077DE	E761 0000 0806		00000000	5742+	LGF	R1, V2ADDR	load v2 source
000077E4	E310 5028 0014		00000028	5743+	VL	v22, 0(R1)	use v21 to test decoder
000077EA	E771 0000 0806		00000000	5744+	LGF	R1, V3ADDR	load v3 source
000077F0	E756 7010 2EF9			5745+	VL	v23, 0(R1)	use v22 to test decoder
000077F6	B98D 0020			5746+	VCHL	V21, V22, V23, 2, 1	test instruction
000077FA	5020 500C		0000000C	5747+	EPSW	R2, R0	extract psw
000077FE	E750 5048 080E		000077B8	5748+	ST	R2, CCPSW	to save CC
00007804	07FB			5749+	VST	V21, V10132	save v1 output
00007808				5750+	BR	R11	return
00007808				5751+RE132	DC	0F	V1 for this test
00007808				5752+	DROP	R5	
00007808	00000000 00000000			5753	DC	XL16' 0000000000000000 0000000000000000'	result
00007810	00000000 00000000						
00007818	08090A0B 0C0D0E0F			5754	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00007820	00010203 04050607						
00007828	119911BB F1DD11FF			5755	DC	XL16' 119911BBF1DD11FF 0111023311550677'	v3
00007830	01110233 11550677						
				5756			
				5757 *Doubleword			
00007838				5758	VRR_B	VCHL, 3, 0	
00007838		00007838		5759+	DS	0FD	
00007838	000078A0			5760+	USING	*, R5	base for test data and test routine
0000783C	0085			5761+T133	DC	A(X133)	address of test routine
0000783E	00			5762+	DC	H' 133'	test number
0000783F	03			5763+	DC	X' 00'	
00007840	01			5764+	DC	HL1' 3'	m4 used
00007841	00			5765+	DC	HL1' 1'	m5 used
00007842	07			5766+	DC	HL1' 0'	CC
00007844	00000000 00000000			5767+	DC	HL1' 7'	CC failed mask
0000784C	FF			5768+	DS	2F	extracted PSW after test (has CC)
0000784D	E5C3C8D3 40404040			5769+	DC	X' FF'	extracted CC, if test failed
00007858	000078D0			5770+	DC	CL8' VCHL'	instruction name
0000785C	000078E0			5771+	DC	A(RE133)	address of v1 result
00007860	000078F0			5772+	DC	A(RE133+16)	address of v2 source
00007864	00000010			5773+	DC	A(RE133+32)	address of v3 source
00007868	000078D0			5774+	DC	A(16)	result length
00007870	00000000 00000000			5775+REA133	DC	A(RE133)	result address
00007878	00000000 00000000			5776+	DS	2FD	gap
00007880	00000000 00000000			5777+V10133	DS	XL16	V1 output
00007888	00000000 00000000						
00007890	00000000 00000000			5778+	DS	2FD	gap
00007898	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000078A0				5779+*			
000078A0	E310 5024 0014		00000024	5780+X133	DS	0F	
000078A6	E761 0000 0806		00000000	5781+	LGF	R1, V2ADDR	load v2 source
000078AC	E310 5028 0014		00000028	5782+	VL	v22, 0(R1)	use v21 to test decoder
000078B2	E771 0000 0806		00000000	5783+	LGF	R1, V3ADDR	load v3 source
000078B8	E756 7010 3EF9			5784+	VL	v23, 0(R1)	use v22 to test decoder
000078BE	B98D 0020			5785+	VCHL	V21, V22, V23, 3, 1	test instruction
000078C2	5020 500C		0000000C	5786+	EPSW	R2, R0	extract psw
000078C6	E750 5048 080E		00007880	5787+	ST	R2, CCPSW	to save CC
000078CC	07FB			5788+	VST	V21, V10133	save v1 output
000078D0				5789+	BR	R11	return
000078D0				5790+RE133	DC	0F	V1 for this test
000078D0	FFFFFFFF FFFFFFFF			5791+	DROP	R5	
000078D0	FFFFFFFF FFFFFFFF			5792	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000078D8	FFFFFFFF FFFFFFFF						
000078E0	01020304 05060708			5793	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
000078E8	090A0B0C 0D0E0F10						
000078F0	00010203 04050607			5794	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
000078F8	08090A0B 0C0D0E0F						
00007900				5795			
00007900		00007900		5796	VRR_B	VCHL, 3, 0	
00007900	00007968			5797+	DS	0FD	
00007904	0086			5798+	USING	*, R5	base for test data and test routine
00007906	00			5799+T134	DC	A(X134)	address of test routine
00007907	03			5800+	DC	H' 134'	test number
00007908	01			5801+	DC	X' 00'	
00007909	00			5802+	DC	HL1' 3'	m4 used
0000790A	07			5803+	DC	HL1' 1'	m5 used
0000790C	00000000 00000000			5804+	DC	HL1' 0'	CC
00007914	FF			5805+	DC	HL1' 7'	CC failed mask
00007915	E5C3C8D3 40404040			5806+	DS	2F	extracted PSW after test (has CC)
00007920	00007998			5807+	DC	X' FF'	extracted CC, if test failed
00007924	000079A8			5808+	DC	CL8' VCHL'	instruction name
00007928	000079B8			5809+	DC	A(RE134)	address of v1 result
0000792C	00000010			5810+	DC	A(RE134+16)	address of v2 source
00007930	00007998			5811+	DC	A(RE134+32)	address of v3 source
00007938	00000000 00000000			5812+	DC	A(16)	result length
00007940	00000000 00000000			5813+REA134	DC	A(RE134)	result address
00007948	00000000 00000000			5814+	DS	2FD	gap
00007950	00000000 00000000			5815+V10134	DS	XL16	V1 output
00007958	00000000 00000000			5816+	DS	2FD	gap
00007960	00000000 00000000						
00007968				5817+*			
00007968	E310 5024 0014		00000024	5818+X134	DS	0F	
0000796E	E761 0000 0806		00000000	5819+	LGF	R1, V2ADDR	load v2 source
00007974	E310 5028 0014		00000028	5820+	VL	v22, 0(R1)	use v21 to test decoder
0000797A	E771 0000 0806		00000000	5821+	LGF	R1, V3ADDR	load v3 source
00007980	E756 7010 3EF9			5822+	VL	v23, 0(R1)	use v22 to test decoder
00007986	B98D 0020			5823+	VCHL	V21, V22, V23, 3, 1	test instruction
0000798A	5020 500C		0000000C	5824+	EPSW	R2, R0	extract psw
0000798E	E750 5048 080E		00007948	5825+	ST	R2, CCPSW	to save CC
00007994	07FB			5826+	VST	V21, V10134	save v1 output
00007998				5827+	BR	R11	return
				5828+RE134	DC	0F	V1 for this test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007998				5829+	DROP R5		
00007998	FFFFFFFF FFFFFFFF			5830	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
000079A0	FFFFFFFF FFFFFFFF						
000079A8	FFFEFFFD FFFCFFFB			5831	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
000079B0	FFFAFFF9 FFF8FFF7						
000079B8	00010203 04050607			5832	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
000079C0	08090A0B 0C0D0E0F						
				5833			
				5834	VRR_B VCHL, 3, 1		
000079C8				5835+	DS	0FD	
000079C8		000079C8		5836+	USING	*, R5	base for test data and test routine
000079C8	00007A30			5837+T135	DC	A(X135)	address of test routine
000079CC	0087			5838+	DC	H' 135'	test number
000079CE	00			5839+	DC	X' 00'	
000079CF	03			5840+	DC	HL1' 3'	m4 used
000079D0	01			5841+	DC	HL1' 1'	m5 used
000079D1	01			5842+	DC	HL1' 1'	CC
000079D2	0B			5843+	DC	HL1' 11'	CC failed mask
000079D4	00000000 00000000			5844+	DS	2F	extracted PSW after test (has CC)
000079DC	FF			5845+	DC	X' FF'	extracted CC, if test failed
000079DD	E5C3C8D3 40404040			5846+	DC	CL8' VCHL'	instruction name
000079E8	00007A60			5847+	DC	A(RE135)	address of v1 result
000079EC	00007A70			5848+	DC	A(RE135+16)	address of v2 source
000079F0	00007A80			5849+	DC	A(RE135+32)	address of v3 source
000079F4	00000010			5850+	DC	A(16)	result length
000079F8	00007A60			5851+REA135	DC	A(RE135)	result address
00007A00	00000000 00000000			5852+	DS	2FD	gap
00007A08	00000000 00000000						
00007A10	00000000 00000000			5853+V10135	DS	XL16	V1 output
00007A18	00000000 00000000						
00007A20	00000000 00000000			5854+	DS	2FD	gap
00007A28	00000000 00000000						
				5855+*			
00007A30				5856+X135	DS	0F	
00007A30	E310 5024 0014		00000024	5857+	LGF	R1, V2ADDR	load v2 source
00007A36	E761 0000 0806		00000000	5858+	VL	v22, 0(R1)	use v21 to test decoder
00007A3C	E310 5028 0014		00000028	5859+	LGF	R1, V3ADDR	load v3 source
00007A42	E771 0000 0806		00000000	5860+	VL	v23, 0(R1)	use v22 to test decoder
00007A48	E756 7010 3EF9			5861+	VCHL	V21, V22, V23, 3, 1	test instruction
00007A4E	B98D 0020			5862+	EPSW	R2, R0	extract psw
00007A52	5020 500C		0000000C	5863+	ST	R2, CCPSW	to save CC
00007A56	E750 5048 080E		00007A10	5864+	VST	V21, V10135	save v1 output
00007A5C	07FB			5865+	BR	R11	return
00007A60				5866+RE135	DC	0F	V1 for this test
00007A60				5867+	DROP	R5	
00007A60	FFFFFFFF FFFFFFFF			5868	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
00007A68	00000000 00000000						
00007A70	00110033 00550077			5869	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v2
00007A78	08090A0B 0C0DFE0F						
00007A80	00010023 00450067			5870	DC	XL16' 0001002300450067 08090A0B0C0DFE1F'	v3
00007A88	08090A0B 0C0DFE1F						
				5871			
				5872	VRR_B VCHL, 3, 1		
00007A90				5873+	DS	0FD	
00007A90		00007A90		5874+	USING	*, R5	base for test data and test routine
00007A90	00007AF8			5875+T136	DC	A(X136)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007A94	0088			5876+	DC	H' 136'	test number
00007A96	00			5877+	DC	X' 00'	
00007A97	03			5878+	DC	HL1' 3'	m4 used
00007A98	01			5879+	DC	HL1' 1'	m5 used
00007A99	01			5880+	DC	HL1' 1'	CC
00007A9A	0B			5881+	DC	HL1' 11'	CC failed mask
00007A9C	00000000 00000000			5882+	DS	2F	extracted PSW after test (has CC)
00007AA4	FF			5883+	DC	X' FF'	extracted CC, if test failed
00007AA5	E5C3C8D3 40404040			5884+	DC	CL8' VCHL'	instruction name
00007AB0	00007B28			5885+	DC	A(RE136)	address of v1 result
00007AB4	00007B38			5886+	DC	A(RE136+16)	address of v2 source
00007AB8	00007B48			5887+	DC	A(RE136+32)	address of v3 source
00007ABC	00000010			5888+	DC	A(16)	result length
00007AC0	00007B28			5889+REA136	DC	A(RE136)	result address
00007AC8	00000000 00000000			5890+	DS	2FD	gap
00007AD0	00000000 00000000						
00007AD8	00000000 00000000			5891+V10136	DS	XL16	V1 output
00007AE0	00000000 00000000						
00007AE8	00000000 00000000			5892+	DS	2FD	gap
00007AF0	00000000 00000000						
				5893+*			
00007AF8				5894+X136	DS	0F	
00007AF8	E310 5024 0014		00000024	5895+	LGF	R1, V2ADDR	load v2 source
00007AFE	E761 0000 0806		00000000	5896+	VL	v22, 0(R1)	use v21 to test decoder
00007B04	E310 5028 0014		00000028	5897+	LGF	R1, V3ADDR	load v3 source
00007B0A	E771 0000 0806		00000000	5898+	VL	v23, 0(R1)	use v22 to test decoder
00007B10	E756 7010 3EF9			5899+	VCHL	V21, V22, V23, 3, 1	test instruction
00007B16	B98D 0020			5900+	EPSW	R2, R0	extract psw
00007B1A	5020 500C		0000000C	5901+	ST	R2, CCPSW	to save CC
00007B1E	E750 5048 080E		00007AD8	5902+	VST	V21, V10136	save v1 output
00007B24	07FB			5903+	BR	R11	return
00007B28				5904+RE136	DC	0F	V1 for this test
00007B28				5905+	DROP	R5	
00007B28	00000000 00000000			5906	DC	XL16' 0000000000000000 FFFFFFFF'	result t
00007B30	FFFFFFFF FFFFFFFF						
00007B38	08090A0B 0C0DFE0F			5907	DC	XL16' 08090A0B0C0DFE0F 0011003300550077'	v2
00007B40	00110033 00550077						
00007B48	08090A0B 0C0DFE1F			5908	DC	XL16' 08090A0B0C0DFE1F 0001002300450067'	v3
00007B50	00010023 00450067						
				5909			
00007B58				5910	VRR_B	VCHL, 3, 3	
00007B58		00007B58		5911+	DS	0FD	
00007B58	00007BC0			5912+	USING	*, R5	base for test data and test routine
00007B5C	0089			5913+T137	DC	A(X137)	address of test routine
00007B5E	00			5914+	DC	H' 137'	test number
00007B5F	03			5915+	DC	X' 00'	
00007B60	01			5916+	DC	HL1' 3'	m4 used
00007B61	03			5917+	DC	HL1' 1'	m5 used
00007B62	0E			5918+	DC	HL1' 3'	CC
00007B62	0E			5919+	DC	HL1' 14'	CC failed mask
00007B64	00000000 00000000			5920+	DS	2F	extracted PSW after test (has CC)
00007B6C	FF			5921+	DC	X' FF'	extracted CC, if test failed
00007B6D	E5C3C8D3 40404040			5922+	DC	CL8' VCHL'	instruction name
00007B78	00007BF0			5923+	DC	A(RE137)	address of v1 result
00007B7C	00007C00			5924+	DC	A(RE137+16)	address of v2 source
00007B80	00007C10			5925+	DC	A(RE137+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007B84	00000010			5926+	DC	A(16)	result length
00007B88	00007BF0			5927+REA137	DC	A(RE137)	result address
00007B90	00000000 00000000			5928+	DS	2FD	gap
00007B98	00000000 00000000						
00007BA0	00000000 00000000			5929+V10137	DS	XL16	V1 output
00007BA8	00000000 00000000						
00007BB0	00000000 00000000			5930+	DS	2FD	gap
00007BB8	00000000 00000000						
00007BC0				5931+*			
00007BC0	E310 5024 0014		00000024	5932+X137	DS	0F	
00007BC6	E761 0000 0806		00000000	5933+	LGF	R1, V2ADDR	load v2 source
00007BCC	E310 5028 0014		00000028	5934+	VL	v22, 0(R1)	use v21 to test decoder
00007BD2	E771 0000 0806		00000000	5935+	LGF	R1, V3ADDR	load v3 source
00007BD8	E756 7010 3EF9			5936+	VL	v23, 0(R1)	use v22 to test decoder
00007BDE	B98D 0020			5937+	VCHL	V21, V22, V23, 3, 1	test instruction
00007BDE	B98D 0020			5938+	EPSW	R2, R0	extract psw
00007BE2	5020 500C		0000000C	5939+	ST	R2, CCPSW	to save CC
00007BE6	E750 5048 080E		00007BA0	5940+	VST	V21, V10137	save v1 output
00007BEC	07FB			5941+	BR	R11	return
00007BF0				5942+RE137	DC	0F	V1 for this test
00007BF0				5943+	DROP	R5	
00007BF0	00000000 00000000			5944	DC	XL16' 0000000000000000 0000000000000000'	result
00007BF8	00000000 00000000						
00007C00	00010003 04050607			5945	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00007C08	00090A0B 0C0D0E0F						
00007C10	01110233 11550677			5946	DC	XL16' 0111023311550677 119911BBF1DD11FF'	v3
00007C18	119911BB F1DD11FF						
00007C20				5947			
00007C20				5948	VRR_B	VCHL, 3, 3	
00007C20		00007C20		5949+	DS	0FD	
00007C20	00007C88			5950+	USING	*, R5	base for test data and test routine
00007C24	008A			5951+T138	DC	A(X138)	address of test routine
00007C26	00			5952+	DC	H' 138'	test number
00007C26	00			5953+	DC	X' 00'	
00007C27	03			5954+	DC	HL1' 3'	m4 used
00007C28	01			5955+	DC	HL1' 1'	m5 used
00007C29	03			5956+	DC	HL1' 3'	CC
00007C2A	0E			5957+	DC	HL1' 14'	CC failed mask
00007C2C	00000000 00000000			5958+	DS	2F	extracted PSW after test (has CC)
00007C34	FF			5959+	DC	X' FF'	extracted CC, if test failed
00007C35	E5C3C8D3 40404040			5960+	DC	CL8' VCHL'	instruction name
00007C40	00007CB8			5961+	DC	A(RE138)	address of v1 result
00007C44	00007CC8			5962+	DC	A(RE138+16)	address of v2 source
00007C48	00007CD8			5963+	DC	A(RE138+32)	address of v3 source
00007C4C	00000010			5964+	DC	A(16)	result length
00007C50	00007CB8			5965+REA138	DC	A(RE138)	result address
00007C58	00000000 00000000			5966+	DS	2FD	gap
00007C60	00000000 00000000						
00007C68	00000000 00000000			5967+V10138	DS	XL16	V1 output
00007C70	00000000 00000000						
00007C78	00000000 00000000			5968+	DS	2FD	gap
00007C80	00000000 00000000						
00007C88				5969+*			
00007C88	E310 5024 0014		00000024	5970+X138	DS	0F	
00007C8E	E761 0000 0806		00000000	5971+	LGF	R1, V2ADDR	load v2 source
				5972+	VL	v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007C94	E310 5028 0014		00000028	5973+	LGF	R1, V3ADDR	load v3 source
00007C9A	E771 0000 0806		00000000	5974+	VL	v23, 0(R1)	use v22 to test decoder
00007CA0	E756 7010 3EF9			5975+	VCHL	V21, V22, V23, 3, 1	test instruction
00007CA6	B98D 0020			5976+	EPSW	R2, R0	extract psw
00007CAA	5020 500C		0000000C	5977+	ST	R2, CCPSW	to save CC
00007CAE	E750 5048 080E		00007C68	5978+	VST	V21, V10138	save v1 output
00007CB4	07FB			5979+	BR	R11	return
00007CB8				5980+RE138	DC	0F	V1 for this test
00007CB8				5981+	DROP	R5	
00007CB8	00000000 00000000			5982	DC	XL16' 0000000000000000 0000000000000000'	result t
00007CC0	00000000 00000000						
00007CC8	08090A0B 0C0D0E0F			5983	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00007CD0	00010203 04050607						
00007CD8	119911BB F1DD11FF			5984	DC	XL16' 119911BBF1DD11FF 0111023311550677'	v3
00007CE0	01110233 11550677						
				5985			
				5986 *			
				5987 * VCH		- Vector Compare High	
				5988 *			
				5989 *		cc=0: All elements high	
				5990 *		cc=1: Some elements high	
				5991 *		cc=3: No element high	
				5992 *			
				5993 *		case - simple cc debug	
				5994 *			
				5995 *		Byte	
				5996	VRR_B	VCH, 0, 0	
00007CE8				5997+	DS	0FD	
00007CE8		00007CE8		5998+	USING	*, R5	base for test data and test routine
00007CE8	00007D50			5999+T139	DC	A(X139)	address of test routine
00007CEC	008B			6000+	DC	H' 139'	test number
00007CEE	00			6001+	DC	X' 00'	
00007CEF	00			6002+	DC	HL1' 0'	m4 used
00007CF0	01			6003+	DC	HL1' 1'	m5 used
00007CF1	00			6004+	DC	HL1' 0'	CC
00007CF2	07			6005+	DC	HL1' 7'	CC failed mask
00007CF4	00000000 00000000			6006+	DS	2F	extracted PSW after test (has CC)
00007CFC	FF			6007+	DC	X' FF'	extracted CC, if test failed
00007CFD	E5C3C840 40404040			6008+	DC	CL8' VCH'	instruction name
00007D08	00007D80			6009+	DC	A(RE139)	address of v1 result
00007D0C	00007D90			6010+	DC	A(RE139+16)	address of v2 source
00007D10	00007DA0			6011+	DC	A(RE139+32)	address of v3 source
00007D14	00000010			6012+	DC	A(16)	result length
00007D18	00007D80			6013+REA139	DC	A(RE139)	result address
00007D20	00000000 00000000			6014+	DS	2FD	gap
00007D28	00000000 00000000						
00007D30	00000000 00000000			6015+V10139	DS	XL16	V1 output
00007D38	00000000 00000000						
00007D40	00000000 00000000			6016+	DS	2FD	gap
00007D48	00000000 00000000						
				6017+*			
00007D50				6018+X139	DS	0F	
00007D50	E310 5024 0014		00000024	6019+	LGF	R1, V2ADDR	load v2 source
00007D56	E761 0000 0806		00000000	6020+	VL	v22, 0(R1)	use v21 to test decoder
00007D5C	E310 5028 0014		00000028	6021+	LGF	R1, V3ADDR	load v3 source
00007D62	E771 0000 0806		00000000	6022+	VL	v23, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00007D68	E756 7010 0EFB			6023+	VCH	V21, V22, V23, 0, 1	test instruction
00007D6E	B98D 0020			6024+	EPSW	R2, R0	extract psw
00007D72	5020 500C		0000000C	6025+	ST	R2, CCPSW	to save CC
00007D76	E750 5048 080E		00007D30	6026+	VST	V21, V10139	save v1 output
00007D7C	07FB			6027+	BR	R11	return
00007D80				6028+RE139	DC	0F	V1 for this test
00007D80				6029+	DROP	R5	
00007D80	FFFFFFFF FFFFFFFF			6030	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00007D88	FFFFFFFF FFFFFFFF						
00007D90	00000000 00000000			6031	DC	XL16' 0000000000000000 0000000000000000'	v2
00007D98	00000000 00000000						
00007DA0	FFFFFFFF FFFFFFFF			6032	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00007DA8	FFFFFFFF FFFFFFFF						
				6033			
00007DB0				6034	VRR_B	VCH, 0, 1	
00007DB0		00007DB0		6035+	DS	0FD	
00007DB0	00007E18			6036+	USING	*, R5	base for test data and test routine
00007DB4	008C			6037+T140	DC	A(X140)	address of test routine
00007DB6	00			6038+	DC	H' 140'	test number
00007DB7	00			6039+	DC	X' 00'	
00007DB8	01			6040+	DC	HL1' 0'	m4 used
00007DB8	01			6041+	DC	HL1' 1'	m5 used
00007DB9	01			6042+	DC	HL1' 1'	CC
00007DBA	0B			6043+	DC	HL1' 11'	CC failed mask
00007DBC	00000000 00000000			6044+	DS	2F	extracted PSW after test (has CC)
00007DC4	FF			6045+	DC	X' FF'	extracted CC, if test failed
00007DC5	E5C3C840 40404040			6046+	DC	CL8' VCH'	instruction name
00007DD0	00007E48			6047+	DC	A(RE140)	address of v1 result
00007DD4	00007E58			6048+	DC	A(RE140+16)	address of v2 source
00007DD8	00007E68			6049+	DC	A(RE140+32)	address of v3 source
00007DDC	00000010			6050+	DC	A(16)	result length
00007DE0	00007E48			6051+REA140	DC	A(RE140)	result address
00007DE8	00000000 00000000			6052+	DS	2FD	gap
00007DF0	00000000 00000000						
00007DF8	00000000 00000000			6053+V10140	DS	XL16	V1 output
00007E00	00000000 00000000						
00007E08	00000000 00000000			6054+	DS	2FD	gap
00007E10	00000000 00000000						
				6055+*			
00007E18				6056+X140	DS	0F	
00007E18	E310 5024 0014		00000024	6057+	LGF	R1, V2ADDR	load v2 source
00007E1E	E761 0000 0806		00000000	6058+	VL	v22, 0(R1)	use v21 to test decoder
00007E24	E310 5028 0014		00000028	6059+	LGF	R1, V3ADDR	load v3 source
00007E2A	E771 0000 0806		00000000	6060+	VL	v23, 0(R1)	use v22 to test decoder
00007E30	E756 7010 0EFB			6061+	VCH	V21, V22, V23, 0, 1	test instruction
00007E36	B98D 0020			6062+	EPSW	R2, R0	extract psw
00007E3A	5020 500C		0000000C	6063+	ST	R2, CCPSW	to save CC
00007E3E	E750 5048 080E		00007DF8	6064+	VST	V21, V10140	save v1 output
00007E44	07FB			6065+	BR	R11	return
00007E48				6066+RE140	DC	0F	V1 for this test
00007E48				6067+	DROP	R5	
00007E48	00000000 00000000			6068	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result t
00007E50	FFFFFFFF 00000000						
00007E58	00000000 00000000			6069	DC	XL16' 0000000000000000 7F017F0200000000'	v2
00007E60	7F017F02 00000000						
00007E68	00000000 00000000			6070	DC	XL16' 0000000000000000 0000000000000000'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00007E70	00000000 00000000			6071				
				6072	VRR_B	VCH, 0, 3		
00007E78				6073+	DS	0FD		
00007E78		00007E78		6074+	USING	*, R5	base for test data and test routine	
00007E78	00007EE0			6075+T141	DC	A(X141)	address of test routine	
00007E7C	008D			6076+	DC	H' 141'	test number	
00007E7E	00			6077+	DC	X' 00'		
00007E7F	00			6078+	DC	HL1' 0'	m4 used	
00007E80	01			6079+	DC	HL1' 1'	m5 used	
00007E81	03			6080+	DC	HL1' 3'	CC	
00007E82	0E			6081+	DC	HL1' 14'	CC failed mask	
00007E84	00000000 00000000			6082+	DS	2F	extracted PSW after test (has CC)	
00007E8C	FF			6083+	DC	X' FF'	extracted CC, if test failed	
00007E8D	E5C3C840 40404040			6084+	DC	CL8' VCH'	instruction name	
00007E98	00007F10			6085+	DC	A(RE141)	address of v1 result	
00007E9C	00007F20			6086+	DC	A(RE141+16)	address of v2 source	
00007EA0	00007F30			6087+	DC	A(RE141+32)	address of v3 source	
00007EA4	00000010			6088+	DC	A(16)	result length	
00007EA8	00007F10			6089+REA141	DC	A(RE141)	result address	
00007EB0	00000000 00000000			6090+	DS	2FD	gap	
00007EB8	00000000 00000000							
00007EC0	00000000 00000000			6091+V10141	DS	XL16	V1 output	
00007EC8	00000000 00000000							
00007ED0	00000000 00000000			6092+	DS	2FD	gap	
00007ED8	00000000 00000000							
				6093+*				
00007EE0				6094+X141	DS	0F		
00007EE0	E310 5024 0014		00000024	6095+	LGF	R1, V2ADDR	load v2 source	
00007EE6	E761 0000 0806		00000000	6096+	VL	v22, 0(R1)	use v21 to test decoder	
00007EEC	E310 5028 0014		00000028	6097+	LGF	R1, V3ADDR	load v3 source	
00007EF2	E771 0000 0806		00000000	6098+	VL	v23, 0(R1)	use v22 to test decoder	
00007EF8	E756 7010 0EFB			6099+	VCH	V21, V22, V23, 0, 1	test instruction	
00007EFE	B98D 0020			6100+	EPSW	R2, R0	extract psw	
00007F02	5020 500C		0000000C	6101+	ST	R2, CCPSW	to save CC	
00007F06	E750 5048 080E		00007EC0	6102+	VST	V21, V10141	save v1 output	
00007F0C	07FB			6103+	BR	R11	return	
00007F10				6104+RE141	DC	0F	V1 for this test	
00007F10				6105+	DROP	R5		
00007F10	00000000 00000000			6106	DC	XL16' 0000000000000000 0000000000000000'	result t	
00007F18	00000000 00000000							
00007F20	00000000 00000000			6107	DC	XL16' 0000000000000000 0000000000000000'	v2	
00007F28	00000000 00000000							
00007F30	00000000 00000000			6108	DC	XL16' 0000000000000000 0000000000000000'	v3	
00007F38	00000000 00000000							
				6109				
				6110 *Hal fword				
				6111	VRR_B	VCH, 1, 0		
00007F40				6112+	DS	0FD		
00007F40		00007F40		6113+	USING	*, R5	base for test data and test routine	
00007F40	00007FA8			6114+T142	DC	A(X142)	address of test routine	
00007F44	008E			6115+	DC	H' 142'	test number	
00007F46	00			6116+	DC	X' 00'		
00007F47	01			6117+	DC	HL1' 1'	m4 used	
00007F48	01			6118+	DC	HL1' 1'	m5 used	
00007F49	00			6119+	DC	HL1' 0'	CC	

LOC	OBJECT CODE			ADDR1	ADDR2	STMT			
00007F4A	07					6120+	DC	HL1' 7'	CC failed mask
00007F4C	00000000	00000000				6121+	DS	2F	extracted PSW after test (has CC)
00007F54	FF					6122+	DC	X' FF'	extracted CC, if test failed
00007F55	E5C3C840	40404040				6123+	DC	CL8' VCH'	instruction name
00007F60	00007FD8					6124+	DC	A(RE142)	address of v1 result
00007F64	00007FE8					6125+	DC	A(RE142+16)	address of v2 source
00007F68	00007FF8					6126+	DC	A(RE142+32)	address of v3 source
00007F6C	00000010					6127+	DC	A(16)	result length
00007F70	00007FD8					6128+REA142	DC	A(RE142)	result address
00007F78	00000000	00000000				6129+	DS	2FD	gap
00007F80	00000000	00000000							
00007F88	00000000	00000000				6130+V10142	DS	XL16	V1 output
00007F90	00000000	00000000							
00007F98	00000000	00000000				6131+	DS	2FD	gap
00007FA0	00000000	00000000							
						6132+*			
00007FA8						6133+X142	DS	0F	
00007FA8	E310 5024 0014			00000024		6134+	LGF	R1, V2ADDR	load v2 source
00007FAE	E761 0000 0806			00000000		6135+	VL	v22, 0(R1)	use v21 to test decoder
00007FB4	E310 5028 0014			00000028		6136+	LGF	R1, V3ADDR	load v3 source
00007FBA	E771 0000 0806			00000000		6137+	VL	v23, 0(R1)	use v22 to test decoder
00007FC0	E756 7010 1EFB					6138+	VCH	V21, V22, V23, 1, 1	test instruction
00007FC6	B98D 0020					6139+	EPSW	R2, R0	extract psw
00007FCA	5020 500C			0000000C		6140+	ST	R2, CCPSW	to save CC
00007FCE	E750 5048 080E			00007F88		6141+	VST	V21, V10142	save v1 output
00007FD4	07FB					6142+	BR	R11	return
00007FD8						6143+RE142	DC	0F	V1 for this test
00007FD8						6144+	DROP	R5	
00007FD8	FFFFFFFF	FFFFFFFF				6145	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00007FE0	FFFFFFFF	FFFFFFFF							
00007FE8	00000000	00000000				6146	DC	XL16' 0000000000000000 0000000000000000'	v2
00007FF0	00000000	00000000							
00007FF8	FFFFFFFF	FFFFFFFF				6147	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00008000	FFFFFFFF	FFFFFFFF							
						6148			
						6149	VRR_B	VCH, 1, 1	
00008008						6150+	DS	0FD	
00008008			00008008			6151+	USING	*, R5	base for test data and test routine
00008008	00008070					6152+T143	DC	A(X143)	address of test routine
0000800C	008F					6153+	DC	H' 143'	test number
0000800E	00					6154+	DC	X' 00'	
0000800F	01					6155+	DC	HL1' 1'	m4 used
00008010	01					6156+	DC	HL1' 1'	m5 used
00008011	01					6157+	DC	HL1' 1'	CC
00008012	0B					6158+	DC	HL1' 11'	CC failed mask
00008014	00000000	00000000				6159+	DS	2F	extracted PSW after test (has CC)
0000801C	FF					6160+	DC	X' FF'	extracted CC, if test failed
0000801D	E5C3C840	40404040				6161+	DC	CL8' VCH'	instruction name
00008028	000080A0					6162+	DC	A(RE143)	address of v1 result
0000802C	000080B0					6163+	DC	A(RE143+16)	address of v2 source
00008030	000080C0					6164+	DC	A(RE143+32)	address of v3 source
00008034	00000010					6165+	DC	A(16)	result length
00008038	000080A0					6166+REA143	DC	A(RE143)	result address
00008040	00000000	00000000				6167+	DS	2FD	gap
00008048	00000000	00000000							
00008050	00000000	00000000				6168+V10143	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008058	00000000 00000000						
00008060	00000000 00000000			6169+	DS	2FD	gap
00008068	00000000 00000000						
00008070				6170+*			
00008070	E310 5024 0014		00000024	6171+X143	DS	0F	
00008076	E761 0000 0806		00000000	6172+	LGF	R1, V2ADDR	load v2 source
0000807C	E310 5028 0014		00000028	6173+	VL	v22, 0(R1)	use v21 to test decoder
00008082	E771 0000 0806		00000000	6174+	LGF	R1, V3ADDR	load v3 source
00008088	E756 7010 1EFB		00000000	6175+	VL	v23, 0(R1)	use v22 to test decoder
0000808E	B98D 0020			6176+	VCH	V21, V22, V23, 1, 1	test instruction
00008092	5020 500C		0000000C	6177+	EPSW	R2, R0	extract psw
00008096	E750 5048 080E		00008050	6178+	ST	R2, CCPSW	to save CC
0000809C	07FB			6179+	VST	V21, V10143	save v1 output
000080A0				6180+	BR	R11	return
000080A0				6181+RE143	DC	0F	V1 for this test
000080A0	00000000 00000000			6182+	DROP	R5	
000080A8	FFFFFFFF 00000000			6183	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result
000080B0	00000000 00000000			6184	DC	XL16' 0000000000000000 7F017F0200000000'	v2
000080B8	7F017F02 00000000						
000080C0	00000000 00000000			6185	DC	XL16' 0000000000000000 0000000000000000'	v3
000080C8	00000000 00000000						
000080D0				6186			
000080D0		000080D0		6187	VRR_B	VCH, 1, 3	
000080D0	00008138			6188+	DS	0FD	
000080D4	0090			6189+	USING	*, R5	base for test data and test routine
000080D6	00			6190+T144	DC	A(X144)	address of test routine
000080D7	01			6191+	DC	H' 144'	test number
000080D8	01			6192+	DC	X' 00'	
000080D9	03			6193+	DC	HL1' 1'	m4 used
000080DA	0E			6194+	DC	HL1' 1'	m5 used
000080DC	00000000 00000000			6195+	DC	HL1' 3'	CC
000080E4	FF			6196+	DC	HL1' 14'	CC failed mask
000080E5	E5C3C840 40404040			6197+	DS	2F	extracted PSW after test (has CC)
000080F0	00008168			6198+	DC	X' FF'	extracted CC, if test failed
000080F4	00008178			6199+	DC	CL8' VCH'	instruction name
000080F8	00008188			6200+	DC	A(RE144)	address of v1 result
000080FC	00000010			6201+	DC	A(RE144+16)	address of v2 source
00008100	00008168			6202+	DC	A(RE144+32)	address of v3 source
00008108	00000000 00000000			6203+	DC	A(16)	result length
00008110	00000000 00000000			6204+REA144	DC	A(RE144)	result address
00008118	00000000 00000000			6205+	DS	2FD	gap
00008120	00000000 00000000			6206+V10144	DS	XL16	V1 output
00008128	00000000 00000000						
00008130	00000000 00000000			6207+	DS	2FD	gap
00008138				6208+*			
00008138	E310 5024 0014		00000024	6209+X144	DS	0F	
0000813E	E761 0000 0806		00000000	6210+	LGF	R1, V2ADDR	load v2 source
00008144	E310 5028 0014		00000028	6211+	VL	v22, 0(R1)	use v21 to test decoder
0000814A	E771 0000 0806		00000000	6212+	LGF	R1, V3ADDR	load v3 source
00008150	E756 7010 1EFB			6213+	VL	v23, 0(R1)	use v22 to test decoder
00008156	B98D 0020			6214+	VCH	V21, V22, V23, 1, 1	test instruction
0000815A	5020 500C		0000000C	6215+	EPSW	R2, R0	extract psw
				6216+	ST	R2, CCPSW	to save CC

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000815E	E750 5048 080E		00008118	6217+	VST	V21, V10144	save v1 output
00008164	07FB			6218+	BR	R11	return
00008168				6219+RE144	DC	0F	V1 for this test
00008168				6220+	DROP	R5	
00008168	00000000 00000000			6221	DC	XL16' 0000000000000000 0000000000000000'	result
00008170	00000000 00000000						
00008178	00000000 00000000			6222	DC	XL16' 0000000000000000 0000000000000000'	v2
00008180	00000000 00000000						
00008188	00000000 00000000			6223	DC	XL16' 0000000000000000 0000000000000000'	v3
00008190	00000000 00000000						
				6224			
				6225 *Word			
				6226	VRR_B	VCH, 2, 0	
00008198				6227+	DS	0FD	
00008198		00008198		6228+	USING	*, R5	base for test data and test routine
00008198	00008200			6229+T145	DC	A(X145)	address of test routine
0000819C	0091			6230+	DC	H' 145'	test number
0000819E	00			6231+	DC	X' 00'	
0000819F	02			6232+	DC	HL1' 2'	m4 used
000081A0	01			6233+	DC	HL1' 1'	m5 used
000081A1	00			6234+	DC	HL1' 0'	CC
000081A2	07			6235+	DC	HL1' 7'	CC failed mask
000081A4	00000000 00000000			6236+	DS	2F	extracted PSW after test (has CC)
000081AC	FF			6237+	DC	X' FF'	extracted CC, if test failed
000081AD	E5C3C840 40404040			6238+	DC	CL8' VCH'	instruction name
000081B8	00008230			6239+	DC	A(RE145)	address of v1 result
000081BC	00008240			6240+	DC	A(RE145+16)	address of v2 source
000081C0	00008250			6241+	DC	A(RE145+32)	address of v3 source
000081C4	00000010			6242+	DC	A(16)	result length
000081C8	00008230			6243+REA145	DC	A(RE145)	result address
000081D0	00000000 00000000			6244+	DS	2FD	gap
000081D8	00000000 00000000						
000081E0	00000000 00000000			6245+V10145	DS	XL16	V1 output
000081E8	00000000 00000000						
000081F0	00000000 00000000			6246+	DS	2FD	gap
000081F8	00000000 00000000						
				6247+*			
00008200				6248+X145	DS	0F	
00008200	E310 5024 0014	00000024		6249+	LGF	R1, V2ADDR	load v2 source
00008206	E761 0000 0806	00000000		6250+	VL	v22, 0(R1)	use v21 to test decoder
0000820C	E310 5028 0014	00000028		6251+	LGF	R1, V3ADDR	load v3 source
00008212	E771 0000 0806	00000000		6252+	VL	v23, 0(R1)	use v22 to test decoder
00008218	E756 7010 2EFB			6253+	VCH	V21, V22, V23, 2, 1	test instruction
0000821E	B98D 0020			6254+	EPSW	R2, R0	extract psw
00008222	5020 500C	0000000C		6255+	ST	R2, CCPSW	to save CC
00008226	E750 5048 080E	000081E0		6256+	VST	V21, V10145	save v1 output
0000822C	07FB			6257+	BR	R11	return
00008230				6258+RE145	DC	0F	V1 for this test
00008230				6259+	DROP	R5	
00008230	FFFFFFFF FFFFFFFF			6260	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00008238	FFFFFFFF FFFFFFFF						
00008240	00000000 00000000			6261	DC	XL16' 0000000000000000 0000000000000000'	v2
00008248	00000000 00000000						
00008250	FFFFFFFF FFFFFFFF			6262	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
00008258	FFFFFFFF FFFFFFFF						
				6263			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008260				6264	VRR_B	VCH, 2, 1	
00008260				6265+	DS	0FD	
00008260		00008260		6266+	USING	*, R5	base for test data and test routine
00008260	000082C8			6267+T146	DC	A(X146)	address of test routine
00008264	0092			6268+	DC	H' 146'	test number
00008266	00			6269+	DC	X' 00'	
00008267	02			6270+	DC	HL1' 2'	m4 used
00008268	01			6271+	DC	HL1' 1'	m5 used
00008269	01			6272+	DC	HL1' 1'	CC
0000826A	0B			6273+	DC	HL1' 11'	CC failed mask
0000826C	00000000 00000000			6274+	DS	2F	extracted PSW after test (has CC)
00008274	FF			6275+	DC	X' FF'	extracted CC, if test failed
00008275	E5C3C840 40404040			6276+	DC	CL8' VCH'	instruction name
00008280	000082F8			6277+	DC	A(RE146)	address of v1 result
00008284	00008308			6278+	DC	A(RE146+16)	address of v2 source
00008288	00008318			6279+	DC	A(RE146+32)	address of v3 source
0000828C	00000010			6280+	DC	A(16)	result length
00008290	000082F8			6281+REA146	DC	A(RE146)	result address
00008298	00000000 00000000			6282+	DS	2FD	gap
000082A0	00000000 00000000						
000082A8	00000000 00000000			6283+V10146	DS	XL16	V1 output
000082B0	00000000 00000000						
000082B8	00000000 00000000			6284+	DS	2FD	gap
000082C0	00000000 00000000						
000082C8				6285+*			
000082C8	E310 5024 0014			6286+X146	DS	0F	
000082CE	E761 0000 0806	00000024		6287+	LGF	R1, V2ADDR	load v2 source
000082D4	E310 5028 0014	00000000		6288+	VL	v22, 0(R1)	use v21 to test decoder
000082DA	E771 0000 0806	00000028		6289+	LGF	R1, V3ADDR	load v3 source
000082E0	E756 7010 2EFB	00000000		6290+	VL	v23, 0(R1)	use v22 to test decoder
000082E6	B98D 0020			6291+	VCH	V21, V22, V23, 2, 1	test instruction
000082EA	5020 500C	0000000C		6292+	EPSW	R2, R0	extract psw
000082EE	E750 5048 080E	000082A8		6293+	ST	R2, CCPSW	to save CC
000082F4	07FB			6294+	VST	V21, V10146	save v1 output
000082F8				6295+	BR	R11	return
000082F8				6296+RE146	DC	0F	V1 for this test
000082F8				6297+	DROP	R5	
000082F8	00000000 00000000			6298	DC	XL16' 0000000000000000 FFFFFFFF00000000'	result
00008300	FFFFFFFF 00000000						
00008308	00000000 00000000			6299	DC	XL16' 0000000000000000 7F017F0200000000'	v2
00008310	7F017F02 00000000						
00008318	00000000 00000000			6300	DC	XL16' 0000000000000000 0000000000000000'	v3
00008320	00000000 00000000						
00008328				6301			
00008328		00008328		6302	VRR_B	VCH, 2, 3	
00008328				6303+	DS	0FD	
00008328	00008390			6304+	USING	*, R5	base for test data and test routine
0000832C	0093			6305+T147	DC	A(X147)	address of test routine
0000832E	00			6306+	DC	H' 147'	test number
0000832E	00			6307+	DC	X' 00'	
0000832F	02			6308+	DC	HL1' 2'	m4 used
00008330	01			6309+	DC	HL1' 1'	m5 used
00008331	03			6310+	DC	HL1' 3'	CC
00008332	0E			6311+	DC	HL1' 14'	CC failed mask
00008334	00000000 00000000			6312+	DS	2F	extracted PSW after test (has CC)
0000833C	FF			6313+	DC	X' FF'	extracted CC, if test failed

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000833D	E5C3C840 40404040			6314+	DC	CL8' VCH'	instruction name
00008348	000083C0			6315+	DC	A(RE147)	address of v1 result
0000834C	000083D0			6316+	DC	A(RE147+16)	address of v2 source
00008350	000083E0			6317+	DC	A(RE147+32)	address of v3 source
00008354	00000010			6318+	DC	A(16)	result length
00008358	000083C0			6319+REA147	DC	A(RE147)	result address
00008360	00000000 00000000			6320+	DS	2FD	gap
00008368	00000000 00000000						
00008370	00000000 00000000			6321+V10147	DS	XL16	V1 output
00008378	00000000 00000000						
00008380	00000000 00000000			6322+	DS	2FD	gap
00008388	00000000 00000000						
00008390				6323+*			
00008390	E310 5024 0014		00000024	6324+X147	DS	0F	
00008396	E761 0000 0806		00000000	6325+	LGF	R1, V2ADDR	load v2 source
0000839C	E310 5028 0014		00000028	6326+	VL	v22, 0(R1)	use v21 to test decoder
000083A2	E771 0000 0806		00000000	6327+	LGF	R1, V3ADDR	load v3 source
000083A8	E756 7010 2EFB			6328+	VL	v23, 0(R1)	use v22 to test decoder
000083AE	B98D 0020			6329+	VCH	V21, V22, V23, 2, 1	test instruction
000083B2	5020 500C		0000000C	6330+	EPSW	R2, R0	extract psw
000083B6	E750 5048 080E		00008370	6331+	ST	R2, CCPSW	to save CC
000083BC	07FB			6332+	VST	V21, V10147	save v1 output
000083C0				6333+	BR	R11	return
000083C0				6334+RE147	DC	0F	V1 for this test
000083C0				6335+	DROP	R5	
000083C0	00000000 00000000			6336	DC	XL16' 0000000000000000 0000000000000000'	result t
000083C8	00000000 00000000						
000083D0	00000000 00000000			6337	DC	XL16' 0000000000000000 0000000000000000'	v2
000083D8	00000000 00000000						
000083E0	00000000 00000000			6338	DC	XL16' 0000000000000000 0000000000000000'	v3
000083E8	00000000 00000000						
				6339			
				6340 *Doubleword			
000083F0				6341	VRR_B	VCH, 3, 0	
000083F0		000083F0		6342+	DS	0FD	
000083F0	00008458			6343+	USING	*, R5	base for test data and test routine
000083F4	0094			6344+T148	DC	A(X148)	address of test routine
000083F6	00			6345+	DC	H' 148'	test number
000083F7	03			6346+	DC	X' 00'	
000083F8	01			6347+	DC	HL1' 3'	m4 used
000083F9	00			6348+	DC	HL1' 1'	m5 used
000083FA	07			6349+	DC	HL1' 0'	CC
000083FC	00000000 00000000			6350+	DC	HL1' 7'	CC failed mask
00008404	FF			6351+	DS	2F	extracted PSW after test (has CC)
00008405	E5C3C840 40404040			6352+	DC	X' FF'	extracted CC, if test failed
00008410	00008488			6353+	DC	CL8' VCH'	instruction name
00008414	00008498			6354+	DC	A(RE148)	address of v1 result
00008418	000084A8			6355+	DC	A(RE148+16)	address of v2 source
0000841C	00000010			6356+	DC	A(RE148+32)	address of v3 source
00008420	00008488			6357+	DC	A(16)	result length
00008428	00000000 00000000			6358+REA148	DC	A(RE148)	result address
00008430	00000000 00000000			6359+	DS	2FD	gap
00008438	00000000 00000000			6360+V10148	DS	XL16	V1 output
00008440	00000000 00000000						
00008448	00000000 00000000			6361+	DS	2FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008450	00000000 00000000			6362+*			
00008458				6363+X148	DS	0F	
00008458	E310 5024 0014		00000024	6364+	LGF	R1, V2ADDR	load v2 source
0000845E	E761 0000 0806		00000000	6365+	VL	v22, 0(R1)	use v21 to test decoder
00008464	E310 5028 0014		00000028	6366+	LGF	R1, V3ADDR	load v3 source
0000846A	E771 0000 0806		00000000	6367+	VL	v23, 0(R1)	use v22 to test decoder
00008470	E756 7010 3EFB			6368+	VCH	V21, V22, V23, 3, 1	test instruction
00008476	B98D 0020			6369+	EPSW	R2, R0	extract psw
0000847A	5020 500C		0000000C	6370+	ST	R2, CCPSW	to save CC
0000847E	E750 5048 080E		00008438	6371+	VST	V21, V10148	save v1 output
00008484	07FB			6372+	BR	R11	return
00008488				6373+RE148	DC	0F	V1 for this test
00008488				6374+	DROP	R5	
00008488	FFFFFFFF FFFFFFFF			6375	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00008490	FFFFFFFF FFFFFFFF						
00008498	00000000 00000000			6376	DC	XL16' 0000000000000000 0000000000000000'	v2
000084A0	00000000 00000000						
000084A8	FFFFFFFF FFFFFFFF			6377	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3
000084B0	FFFFFFFF FFFFFFFF						
				6378			
000084B8				6379	VRR_B	VCH, 3, 1	
000084B8		000084B8		6380+	DS	0FD	
000084B8	00008520			6381+	USING	*, R5	base for test data and test routine
000084BC	0095			6382+T149	DC	A(X149)	address of test routine
000084BE	00			6383+	DC	H' 149'	test number
000084BF	03			6384+	DC	X' 00'	
000084C0	01			6385+	DC	HL1' 3'	m4 used
000084C1	01			6386+	DC	HL1' 1'	m5 used
000084C2	0B			6387+	DC	HL1' 1'	CC
000084C2	0B			6388+	DC	HL1' 11'	CC failed mask
000084C4	00000000 00000000			6389+	DS	2F	extracted PSW after test (has CC)
000084CC	FF			6390+	DC	X' FF'	extracted CC, if test failed
000084CD	E5C3C840 40404040			6391+	DC	CL8' VCH'	instruction name
000084D8	00008550			6392+	DC	A(RE149)	address of v1 result
000084DC	00008560			6393+	DC	A(RE149+16)	address of v2 source
000084E0	00008570			6394+	DC	A(RE149+32)	address of v3 source
000084E4	00000010			6395+	DC	A(16)	result length
000084E8	00008550			6396+REA149	DC	A(RE149)	result address
000084F0	00000000 00000000			6397+	DS	2FD	gap
000084F8	00000000 00000000						
00008500	00000000 00000000			6398+V10149	DS	XL16	V1 output
00008508	00000000 00000000						
00008510	00000000 00000000			6399+	DS	2FD	gap
00008518	00000000 00000000						
				6400+*			
00008520				6401+X149	DS	0F	
00008520	E310 5024 0014		00000024	6402+	LGF	R1, V2ADDR	load v2 source
00008526	E761 0000 0806		00000000	6403+	VL	v22, 0(R1)	use v21 to test decoder
0000852C	E310 5028 0014		00000028	6404+	LGF	R1, V3ADDR	load v3 source
00008532	E771 0000 0806		00000000	6405+	VL	v23, 0(R1)	use v22 to test decoder
00008538	E756 7010 3EFB			6406+	VCH	V21, V22, V23, 3, 1	test instruction
0000853E	B98D 0020			6407+	EPSW	R2, R0	extract psw
00008542	5020 500C		0000000C	6408+	ST	R2, CCPSW	to save CC
00008546	E750 5048 080E		00008500	6409+	VST	V21, V10149	save v1 output
0000854C	07FB			6410+	BR	R11	return

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT			
00008550					6411+RE149	DC	0F	V1 for this test
00008550					6412+	DROP	R5	
00008550	00000000	00000000			6413	DC	XL16' 0000000000000000 0000000000000000	result t
00008558	FFFFFFFF	FFFFFFFF						
00008560	00000000	00000000			6414	DC	XL16' 0000000000000000 7F017F0200000000	v2
00008568	7F017F02	00000000						
00008570	00000000	00000000			6415	DC	XL16' 0000000000000000 0000000000000000	v3
00008578	00000000	00000000						
					6416			
00008580					6417	VRR_B	VCH, 3, 3	
00008580			00008580		6418+	DS	0FD	
00008580	000085E8				6419+	USING	*, R5	base for test data and test routine
00008584	0096				6420+T150	DC	A(X150)	address of test routine
00008586	00				6421+	DC	H' 150'	test number
00008587	03				6422+	DC	X' 00'	
00008588	01				6423+	DC	HL1' 3'	m4 used
00008589	03				6424+	DC	HL1' 1'	m5 used
0000858A	0E				6425+	DC	HL1' 3'	CC
0000858C	00000000	00000000			6426+	DC	HL1' 14'	CC failed mask
00008594	FF				6427+	DS	2F	extracted PSW after test (has CC)
00008595	E5C3C840	40404040			6428+	DC	X' FF'	extracted CC, if test failed
000085A0	00008618				6429+	DC	CL8' VCH'	instruction name
000085A4	00008628				6430+	DC	A(RE150)	address of v1 result
000085A8	00008638				6431+	DC	A(RE150+16)	address of v2 source
000085AC	00000010				6432+	DC	A(RE150+32)	address of v3 source
000085B0	00008618				6433+	DC	A(16)	result length
000085B8	00000000	00000000			6434+REA150	DC	A(RE150)	result address
000085C0	00000000	00000000			6435+	DS	2FD	gap
000085C8	00000000	00000000			6436+V10150	DS	XL16	V1 output
000085D0	00000000	00000000						
000085D8	00000000	00000000			6437+	DS	2FD	gap
000085E0	00000000	00000000						
					6438+*			
000085E8					6439+X150	DS	0F	
000085E8	E310 5024 0014		00000024		6440+	LGF	R1, V2ADDR	load v2 source
000085EE	E761 0000 0806		00000000		6441+	VL	v22, 0(R1)	use v21 to test decoder
000085F4	E310 5028 0014		00000028		6442+	LGF	R1, V3ADDR	load v3 source
000085FA	E771 0000 0806		00000000		6443+	VL	v23, 0(R1)	use v22 to test decoder
00008600	E756 7010 3EFB				6444+	VCH	V21, V22, V23, 3, 1	test instruction
00008606	B98D 0020				6445+	EPSW	R2, R0	extract psw
0000860A	5020 500C		0000000C		6446+	ST	R2, CCPSW	to save CC
0000860E	E750 5048 080E		000085C8		6447+	VST	V21, V10150	save v1 output
00008614	07FB				6448+	BR	R11	return
00008618					6449+RE150	DC	0F	V1 for this test
00008618					6450+	DROP	R5	
00008618	00000000	00000000			6451	DC	XL16' 0000000000000000 0000000000000000	result t
00008620	00000000	00000000						
00008628	00000000	00000000			6452	DC	XL16' 0000000000000000 0000000000000000	v2
00008630	00000000	00000000						
00008638	00000000	00000000			6453	DC	XL16' 0000000000000000 0000000000000000	v3
00008640	00000000	00000000						
					6454			
					6455 *			
					6456 *	case -	general	
					6457 *			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				6458 *Byte			
				6459	VRR_B	VCH, 0, 0	
00008648				6460+	DS	0FD	
00008648		00008648		6461+	USING	*, R5	base for test data and test routine
00008648	000086B0			6462+T151	DC	A(X151)	address of test routine
0000864C	0097			6463+	DC	H' 151'	test number
0000864E	00			6464+	DC	X' 00'	
0000864F	00			6465+	DC	HL1' 0'	m4 used
00008650	01			6466+	DC	HL1' 1'	m5 used
00008651	00			6467+	DC	HL1' 0'	CC
00008652	07			6468+	DC	HL1' 7'	CC failed mask
00008654	00000000 00000000			6469+	DS	2F	extracted PSW after test (has CC)
0000865C	FF			6470+	DC	X' FF'	extracted CC, if test failed
0000865D	E5C3C840 40404040			6471+	DC	CL8' VCH'	instruction name
00008668	000086E0			6472+	DC	A(RE151)	address of v1 result
0000866C	000086F0			6473+	DC	A(RE151+16)	address of v2 source
00008670	00008700			6474+	DC	A(RE151+32)	address of v3 source
00008674	00000010			6475+	DC	A(16)	result length
00008678	000086E0			6476+REA151	DC	A(RE151)	result address
00008680	00000000 00000000			6477+	DS	2FD	gap
00008688	00000000 00000000						
00008690	00000000 00000000			6478+V10151	DS	XL16	V1 output
00008698	00000000 00000000						
000086A0	00000000 00000000			6479+	DS	2FD	gap
000086A8	00000000 00000000						
				6480+*			
000086B0				6481+X151	DS	0F	
000086B0	E310 5024 0014		00000024	6482+	LGF	R1, V2ADDR	load v2 source
000086B6	E761 0000 0806		00000000	6483+	VL	v22, 0(R1)	use v21 to test decoder
000086BC	E310 5028 0014		00000028	6484+	LGF	R1, V3ADDR	load v3 source
000086C2	E771 0000 0806		00000000	6485+	VL	v23, 0(R1)	use v22 to test decoder
000086C8	E756 7010 0EFB			6486+	VCH	V21, V22, V23, 0, 1	test instruction
000086CE	B98D 0020			6487+	EPSW	R2, R0	extract psw
000086D2	5020 500C		0000000C	6488+	ST	R2, CCPSW	to save CC
000086D6	E750 5048 080E		00008690	6489+	VST	V21, V10151	save v1 output
000086DC	07FB			6490+	BR	R11	return
000086E0				6491+RE151	DC	0F	V1 for this test
000086E0				6492+	DROP	R5	
000086E0	FFFFFFFF FFFFFFFF			6493	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000086E8	FFFFFFFF FFFFFFFF						
000086F0	01020304 05060708			6494	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
000086F8	090A0B0C 0D0E0F10						
00008700	00010203 04050607			6495	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00008708	08090A0B 0C0D0E0F						
				6496			
				6497	VRR_B	VCH, 0, 0	
00008710				6498+	DS	0FD	
00008710		00008710		6499+	USING	*, R5	base for test data and test routine
00008710	00008778			6500+T152	DC	A(X152)	address of test routine
00008714	0098			6501+	DC	H' 152'	test number
00008716	00			6502+	DC	X' 00'	
00008717	00			6503+	DC	HL1' 0'	m4 used
00008718	01			6504+	DC	HL1' 1'	m5 used
00008719	00			6505+	DC	HL1' 0'	CC
0000871A	07			6506+	DC	HL1' 7'	CC failed mask
0000871C	00000000 00000000			6507+	DS	2F	extracted PSW after test (has CC)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00008724	FF			6508+	DC	X' FF' extracted CC, if test failed
00008725	E5C3C840 40404040			6509+	DC	CL8' VCH' instruction name
00008730	000087A8			6510+	DC	A(RE152) address of v1 result
00008734	000087B8			6511+	DC	A(RE152+16) address of v2 source
00008738	000087C8			6512+	DC	A(RE152+32) address of v3 source
0000873C	00000010			6513+	DC	A(16) result length
00008740	000087A8			6514+REA152	DC	A(RE152) result address
00008748	00000000 00000000			6515+	DS	2FD gap
00008750	00000000 00000000					
00008758	00000000 00000000			6516+V10152	DS	XL16 V1 output
00008760	00000000 00000000					
00008768	00000000 00000000			6517+	DS	2FD gap
00008770	00000000 00000000					
00008778				6518+*		
00008778	E310 5024 0014		00000024	6519+X152	DS	0F
0000877E	E761 0000 0806		00000000	6520+	LGF	R1, V2ADDR load v2 source
00008784	E310 5028 0014		00000028	6521+	VL	v22, 0(R1) use v21 to test decoder
0000878A	E771 0000 0806		00000000	6522+	LGF	R1, V3ADDR load v3 source
00008790	E756 7010 0EFB			6523+	VL	v23, 0(R1) use v22 to test decoder
00008796	B98D 0020			6524+	VCH	V21, V22, V23, 0, 1 test instruction
0000879A	5020 500C		0000000C	6525+	EPSW	R2, R0 extract psw
0000879E	E750 5048 080E		00008758	6526+	ST	R2, CCPSW to save CC
000087A4	07FB			6527+	VST	V21, V10152 save v1 output
000087A8				6528+	BR	R11 return
000087A8				6529+RE152	DC	0F V1 for this test
000087A8				6530+	DROP	R5
000087A8	FFFFFFFF FFFFFFFF			6531	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF' result t
000087B0	FFFFFFFF FFFFFFFF					
000087B8	00010203 04050607			6532	DC	XL16' 0001020304050607 08090A0B0C0D0E0F' v2
000087C0	08090A0B 0C0D0E0F					
000087C8	FFFEFFFD FFFCFFFB			6533	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7' v3
000087D0	FFFAFFF9 FFF8FFF7					
000087D8				6534		
000087D8				6535	VRR_B	VCH, 0, 1
000087D8	00008840	000087D8		6536+	DS	0FD
000087DC	0099			6537+	USING	*, R5 base for test data and test routine
000087DE	00			6538+T153	DC	A(X153) address of test routine
000087DF	00			6539+	DC	H' 153' test number
000087E0	01			6540+	DC	X' 00'
000087E1	01			6541+	DC	HL1' 0' m4 used
000087E2	0B			6542+	DC	HL1' 1' m5 used
000087E4	00000000 00000000			6543+	DC	HL1' 1' CC
000087EC	FF			6544+	DC	HL1' 11' CC failed mask
000087ED	E5C3C840 40404040			6545+	DS	2F extracted PSW after test (has CC)
000087F8	00008870			6546+	DC	X' FF' extracted CC, if test failed
000087FC	00008880			6547+	DC	CL8' VCH' instruction name
00008800	00008890			6548+	DC	A(RE153) address of v1 result
00008804	00000010			6549+	DC	A(RE153+16) address of v2 source
00008808	00008870			6550+	DC	A(RE153+32) address of v3 source
00008810	00000000 00000000			6551+	DC	A(16) result length
00008818	00000000 00000000			6552+REA153	DC	A(RE153) result address
00008820	00000000 00000000			6553+	DS	2FD gap
00008828	00000000 00000000					
00008830	00000000 00000000			6554+V10153	DS	XL16 V1 output
				6555+	DS	2FD gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008838	00000000 00000000			6556+*			
00008840				6557+X153	DS	0F	
00008840	E310 5024 0014		00000024	6558+	LGF	R1, V2ADDR	load v2 source
00008846	E761 0000 0806		00000000	6559+	VL	v22, 0(R1)	use v21 to test decoder
0000884C	E310 5028 0014		00000028	6560+	LGF	R1, V3ADDR	load v3 source
00008852	E771 0000 0806		00000000	6561+	VL	v23, 0(R1)	use v22 to test decoder
00008858	E756 7010 0EFB			6562+	VCH	V21, V22, V23, 0, 1	test instruction
0000885E	B98D 0020			6563+	EPSW	R2, R0	extract psw
00008862	5020 500C		0000000C	6564+	ST	R2, CCPSW	to save CC
00008866	E750 5048 080E		00008820	6565+	VST	V21, V10153	save v1 output
0000886C	07FB			6566+	BR	R11	return
00008870				6567+RE153	DC	0F	V1 for this test
00008870				6568+	DROP	R5	
00008870	00FF00FF 00FF00FF			6569	DC	XL16' 00FF00FF00FF00FF	00000000000000FF' result t
00008878	00000000 000000FF						
00008880	00110033 00550077			6570	DC	XL16' 0011003300550077	08090A0B0C0DFE1F' v2
00008888	08090A0B 0C0DFE1F						
00008890	00010203 04050607			6571	DC	XL16' 0001020304050607	08090A0B0C0DFE0F' v3
00008898	08090A0B 0C0DFE0F						
				6572			
000088A0				6573	VRR_B	VCH, 0, 1	
000088A0		000088A0		6574+	DS	0FD	
000088A0	00008908			6575+	USING	*, R5	base for test data and test routine
000088A4	009A			6576+T154	DC	A(X154)	address of test routine
000088A6	00			6577+	DC	H' 154'	test number
000088A7	00			6578+	DC	X' 00'	
000088A8	01			6579+	DC	HL1' 0'	m4 used
000088A9	01			6580+	DC	HL1' 1'	m5 used
000088AA	0B			6581+	DC	HL1' 1'	CC
000088AC	00000000 00000000			6582+	DC	HL1' 11'	CC failed mask
000088B4	FF			6583+	DS	2F	extracted PSW after test (has CC)
000088B5	E5C3C840 40404040			6584+	DC	X' FF'	extracted CC, if test failed
000088C0	00008938			6585+	DC	CL8' VCH'	instruction name
000088C4	00008948			6586+	DC	A(RE154)	address of v1 result
000088C8	00008958			6587+	DC	A(RE154+16)	address of v2 source
000088CC	00000010			6588+	DC	A(RE154+32)	address of v3 source
000088D0	00008938			6589+	DC	A(16)	result length
000088D8	00000000 00000000			6590+REA154	DC	A(RE154)	result address
000088E0	00000000 00000000			6591+	DS	2FD	gap
000088E8	00000000 00000000			6592+V10154	DS	XL16	V1 output
000088F0	00000000 00000000						
000088F8	00000000 00000000			6593+	DS	2FD	gap
00008900	00000000 00000000						
				6594+*			
00008908				6595+X154	DS	0F	
00008908	E310 5024 0014		00000024	6596+	LGF	R1, V2ADDR	load v2 source
0000890E	E761 0000 0806		00000000	6597+	VL	v22, 0(R1)	use v21 to test decoder
00008914	E310 5028 0014		00000028	6598+	LGF	R1, V3ADDR	load v3 source
0000891A	E771 0000 0806		00000000	6599+	VL	v23, 0(R1)	use v22 to test decoder
00008920	E756 7010 0EFB			6600+	VCH	V21, V22, V23, 0, 1	test instruction
00008926	B98D 0020			6601+	EPSW	R2, R0	extract psw
0000892A	5020 500C		0000000C	6602+	ST	R2, CCPSW	to save CC
0000892E	E750 5048 080E		000088E8	6603+	VST	V21, V10154	save v1 output
00008934	07FB			6604+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008938				6605+RE154	DC	0F	V1 for this test
00008938				6606+	DROP	R5	
00008938	00000000 000000FF			6607	DC	XL16' 00000000000000FF 00FF00FF00FF00FF'	result
00008940	00FF00FF 00FF00FF						
00008948	08090A0B 0C0DFE1F			6608	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
00008950	00110033 00550077						
00008958	08090A0B 0C0DFE0F			6609	DC	XL16' 08090A0B0C0DFE0F 0001020304050607'	v3
00008960	00010203 04050607						
				6610			
00008968				6611	VRR_B	VCH, 0, 1	
00008968		00008968		6612+	DS	0FD	
00008968	000089D0			6613+	USING	*, R5	base for test data and test routine
0000896C	009B			6614+T155	DC	A(X155)	address of test routine
0000896E	00			6615+	DC	H' 155'	test number
0000896F	00			6616+	DC	X' 00'	
00008970	01			6617+	DC	HL1' 0'	m4 used
00008971	01			6618+	DC	HL1' 1'	m5 used
00008972	0B			6619+	DC	HL1' 1'	CC
00008974	00000000 00000000			6620+	DC	HL1' 11'	CC failed mask
0000897C	FF			6621+	DS	2F	extracted PSW after test (has CC)
0000897D	E5C3C840 40404040			6622+	DC	X' FF'	extracted CC, if test failed
00008988	00008A00			6623+	DC	CL8' VCH'	instruction name
0000898C	00008A10			6624+	DC	A(RE155)	address of v1 result
00008990	00008A20			6625+	DC	A(RE155+16)	address of v2 source
00008994	00000010			6626+	DC	A(RE155+32)	address of v3 source
00008998	00008A00			6627+	DC	A(16)	result length
000089A0	00000000 00000000			6628+REA155	DC	A(RE155)	result address
000089A8	00000000 00000000			6629+	DS	2FD	gap
000089B0	00000000 00000000			6630+V10155	DS	XL16	V1 output
000089B8	00000000 00000000						
000089C0	00000000 00000000			6631+	DS	2FD	gap
000089C8	00000000 00000000						
				6632+*			
000089D0				6633+X155	DS	0F	
000089D0	E310 5024 0014		00000024	6634+	LGF	R1, V2ADDR	load v2 source
000089D6	E761 0000 0806		00000000	6635+	VL	v22, 0(R1)	use v21 to test decoder
000089DC	E310 5028 0014		00000028	6636+	LGF	R1, V3ADDR	load v3 source
000089E2	E771 0000 0806		00000000	6637+	VL	v23, 0(R1)	use v22 to test decoder
000089E8	E756 7010 0EFB			6638+	VCH	V21, V22, V23, 0, 1	test instruction
000089EE	B98D 0020			6639+	EPSW	R2, R0	extract psw
000089F2	5020 500C		0000000C	6640+	ST	R2, CCPSW	to save CC
000089F6	E750 5048 080E		000089B0	6641+	VST	V21, V10155	save v1 output
000089FC	07FB			6642+	BR	R11	return
00008A00				6643+RE155	DC	0F	V1 for this test
00008A00				6644+	DROP	R5	
00008A00	FFFFFFFF FFFFFFFF			6645	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
00008A08	00000000 00000000						
00008A10	00010203 04050607			6646	DC	XL16' 0001020304050607 FFFAFFF9FFF8FFF7'	v2
00008A18	FFFAFFF9 FFF8FFF7						
00008A20	FFFEFFFD FFFCFFFB			6647	DC	XL16' FFFEFFFDFFFCFFFB 08090A0B0C0D0E0F'	v3
00008A28	08090A0B 0C0D0E0F						
				6648			
00008A30				6649	VRR_B	VCH, 0, 3	
00008A30		00008A30		6650+	DS	0FD	
				6651+	USING	*, R5	base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00008A30	00008A98			6652+T156	DC	A(X156) address of test routine
00008A34	009C			6653+	DC	H' 156' test number
00008A36	00			6654+	DC	X' 00'
00008A37	00			6655+	DC	HL1' 0' m4 used
00008A38	01			6656+	DC	HL1' 1' m5 used
00008A39	03			6657+	DC	HL1' 3' CC
00008A3A	0E			6658+	DC	HL1' 14' CC failed mask
00008A3C	00000000 00000000			6659+	DS	2F extracted PSW after test (has CC)
00008A44	FF			6660+	DC	X' FF' extracted CC, if test failed
00008A45	E5C3C840 40404040			6661+	DC	CL8' VCH' instruction name
00008A50	00008AC8			6662+	DC	A(RE156) address of v1 result
00008A54	00008AD8			6663+	DC	A(RE156+16) address of v2 source
00008A58	00008AE8			6664+	DC	A(RE156+32) address of v3 source
00008A5C	00000010			6665+	DC	A(16) result length
00008A60	00008AC8			6666+REA156	DC	A(RE156) result address
00008A68	00000000 00000000			6667+	DS	2FD gap
00008A70	00000000 00000000					
00008A78	00000000 00000000			6668+V10156	DS	XL16 V1 output
00008A80	00000000 00000000					
00008A88	00000000 00000000			6669+	DS	2FD gap
00008A90	00000000 00000000					
00008A98				6670+*		
00008A98	E310 5024 0014		00000024	6671+X156	DS	0F
00008A9E	E761 0000 0806		00000000	6672+	LGF	R1, V2ADDR load v2 source
00008AA4	E310 5028 0014		00000028	6673+	VL	v22, 0(R1) use v21 to test decoder
00008AAA	E771 0000 0806		00000000	6674+	LGF	R1, V3ADDR load v3 source
00008AB0	E756 7010 0EFB			6675+	VL	v23, 0(R1) use v22 to test decoder
00008AB6	B98D 0020			6676+	VCH	V21, V22, V23, 0, 1 test instruction
00008ABA	5020 500C		0000000C	6677+	EPSW	R2, R0 extract psw
00008ABE	E750 5048 080E		00008A78	6678+	ST	R2, CCPSW to save CC
00008AC4	07FB			6679+	VST	V21, V10156 save v1 output
00008AC8				6680+	BR	R11 return
00008AC8				6681+RE156	DC	0F V1 for this test
00008AC8				6682+	DROP	R5
00008AC8	00000000 00000000			6683	DC	XL16' 0000000000000000 0000000000000000' result t
00008AD0	00000000 00000000					
00008AD8	00010003 04050607			6684	DC	XL16' 0001000304050607 00090A0B0C0D0E0F' v2
00008AE0	00090A0B 0C0D0E0F					
00008AE8	01110233 11550677			6685	DC	XL16' 0111023311550677 1179116B514D312F' v3
00008AF0	1179116B 514D312F					
00008AF8				6686		
00008AF8				6687	VRR_B	VCHL, 0, 3
00008AF8		00008AF8		6688+	DS	0FD
00008AF8	00008B60			6689+	USING	*, R5 base for test data and test routine
00008AFC	009D			6690+T157	DC	A(X157) address of test routine
00008AFE	00			6691+	DC	H' 157' test number
00008AFF	00			6692+	DC	X' 00'
00008B00	01			6693+	DC	HL1' 0' m4 used
00008B01	03			6694+	DC	HL1' 1' m5 used
00008B02	0E			6695+	DC	HL1' 3' CC
00008B04	00000000 00000000			6696+	DC	HL1' 14' CC failed mask
00008B0C	FF			6697+	DS	2F extracted PSW after test (has CC)
00008B0D	E5C3C8D3 40404040			6698+	DC	X' FF' extracted CC, if test failed
00008B18	00008B90			6699+	DC	CL8' VCHL' instruction name
00008B1C	00008BA0			6700+	DC	A(RE157) address of v1 result
				6701+	DC	A(RE157+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008B20	00008BB0			6702+	DC	A(RE157+32)	address of v3 source
00008B24	00000010			6703+	DC	A(16)	result length
00008B28	00008B90			6704+REA157	DC	A(RE157)	result address
00008B30	00000000 00000000			6705+	DS	2FD	gap
00008B38	00000000 00000000						
00008B40	00000000 00000000			6706+V10157	DS	XL16	V1 output
00008B48	00000000 00000000						
00008B50	00000000 00000000			6707+	DS	2FD	gap
00008B58	00000000 00000000						
00008B60				6708+*			
00008B60	E310 5024 0014		00000024	6709+X157	DS	0F	
00008B66	E761 0000 0806		00000000	6710+	LGF	R1, V2ADDR	load v2 source
00008B6C	E310 5028 0014		00000028	6711+	VL	v22, 0(R1)	use v21 to test decoder
00008B72	E771 0000 0806		00000000	6712+	LGF	R1, V3ADDR	load v3 source
00008B78	E756 7010 0EF9			6713+	VL	v23, 0(R1)	use v22 to test decoder
00008B7E	B98D 0020			6714+	VCHL	V21, V22, V23, 0, 1	test instruction
00008B82	5020 500C		0000000C	6715+	EPSW	R2, R0	extract psw
00008B86	E750 5048 080E		00008B40	6716+	ST	R2, CCPSW	to save CC
00008B8C	07FB			6717+	VST	V21, V10157	save v1 output
00008B90				6718+	BR	R11	return
00008B90				6719+RE157	DC	0F	V1 for this test
00008B90	00000000 00000000			6720+	DROP	R5	
00008B98	00000000 00000000			6721	DC	XL16' 0000000000000000 0000000000000000'	result t
00008BA0	08090A0B 0C0D0E0F			6722	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00008BA8	00010203 04050607						
00008BB0	1179116B 514D312F			6723	DC	XL16' 1179116B514D312F 0111023311550677'	v3
00008BB8	01110233 11550677						
00008BC0				6724			
00008BC0		00008BC0		6725	VRR_B	VCH, 0, 3	
00008BC0	00008C28			6726+	DS	0FD	
00008BC4	009E			6727+	USING	*, R5	base for test data and test routine
00008BC6	00			6728+T158	DC	A(X158)	address of test routine
00008BC7	00			6729+	DC	H' 158'	test number
00008BC8	01			6730+	DC	X' 00'	
00008BC9	03			6731+	DC	HL1' 0'	m4 used
00008BCA	0E			6732+	DC	HL1' 1'	m5 used
00008BCC	00000000 00000000			6733+	DC	HL1' 3'	CC
00008BD4	FF			6734+	DC	HL1' 14'	CC failed mask
00008BD5	E5C3C840 40404040			6735+	DS	2F	extracted PSW after test (has CC)
00008BE0	00008C58			6736+	DC	X' FF'	extracted CC, if test failed
00008BE4	00008C68			6737+	DC	CL8' VCH'	instruction name
00008BE8	00008C78			6738+	DC	A(RE158)	address of v1 result
00008BEC	00000010			6739+	DC	A(RE158+16)	address of v2 source
00008BF0	00008C58			6740+	DC	A(RE158+32)	address of v3 source
00008BF8	00000000 00000000			6741+	DC	A(16)	result length
00008C00	00000000 00000000			6742+REA158	DC	A(RE158)	result address
00008C08	00000000 00000000			6743+	DS	2FD	gap
00008C10	00000000 00000000						
00008C18	00000000 00000000			6744+V10158	DS	XL16	V1 output
00008C20	00000000 00000000						
00008C28				6745+	DS	2FD	gap
00008C28	E310 5024 0014		00000024	6746+*			
00008C28				6747+X158	DS	0F	
00008C28				6748+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00008C2E	E761 0000 0806		00000000	6749+	VL	v22, 0(R1)	use v21 to test decoder	
00008C34	E310 5028 0014		00000028	6750+	LGF	R1, V3ADDR	load v3 source	
00008C3A	E771 0000 0806		00000000	6751+	VL	v23, 0(R1)	use v22 to test decoder	
00008C40	E756 7010 0EFB			6752+	VCH	V21, V22, V23, 0, 1	test instruction	
00008C46	B98D 0020			6753+	EPSW	R2, R0	extract psw	
00008C4A	5020 500C		0000000C	6754+	ST	R2, CCPSW	to save CC	
00008C4E	E750 5048 080E		00008C08	6755+	VST	V21, V10158	save v1 output	
00008C54	07FB			6756+	BR	R11	return	
00008C58				6757+RE158	DC	0F	V1 for this test	
00008C58				6758+	DROP	R5		
00008C58	00000000 00000000			6759	DC	XL16' 0000000000000000 0000000000000000'	result t	
00008C60	00000000 00000000							
00008C68	FFFEFFFD FFFCFFFB			6760	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2	
00008C70	FFFAFFF9 FFF8FFF7							
00008C78	01110233 11550677			6761	DC	XL16' 0111023311550677 08090A0B0C0D0E0F'	v3	
00008C80	08090A0B 0C0D0E0F							
				6762				
				6763	*Halfword			
				6764	VRR_B	VCH, 1, 0		
00008C88				6765+	DS	0FD		
00008C88		00008C88		6766+	USING	*, R5	base for test data and test routine	
00008C88	00008CF0			6767+T159	DC	A(X159)	address of test routine	
00008C8C	009F			6768+	DC	H' 159'	test number	
00008C8E	00			6769+	DC	X' 00'		
00008C8F	01			6770+	DC	HL1' 1'	m4 used	
00008C90	01			6771+	DC	HL1' 1'	m5 used	
00008C91	00			6772+	DC	HL1' 0'	CC	
00008C92	07			6773+	DC	HL1' 7'	CC failed mask	
00008C94	00000000 00000000			6774+	DS	2F	extracted PSW after test (has CC)	
00008C9C	FF			6775+	DC	X' FF'	extracted CC, if test failed	
00008C9D	E5C3C840 40404040			6776+	DC	CL8' VCH'	instruction name	
00008CA8	00008D20			6777+	DC	A(RE159)	address of v1 result	
00008CAC	00008D30			6778+	DC	A(RE159+16)	address of v2 source	
00008CB0	00008D40			6779+	DC	A(RE159+32)	address of v3 source	
00008CB4	00000010			6780+	DC	A(16)	result length	
00008CB8	00008D20			6781+REA159	DC	A(RE159)	result address	
00008CC0	00000000 00000000			6782+	DS	2FD	gap	
00008CC8	00000000 00000000							
00008CD0	00000000 00000000			6783+V10159	DS	XL16	V1 output	
00008CD8	00000000 00000000							
00008CE0	00000000 00000000			6784+	DS	2FD	gap	
00008CE8	00000000 00000000							
				6785+*				
00008CF0				6786+X159	DS	0F		
00008CF0	E310 5024 0014		00000024	6787+	LGF	R1, V2ADDR	load v2 source	
00008CF6	E761 0000 0806		00000000	6788+	VL	v22, 0(R1)	use v21 to test decoder	
00008CFC	E310 5028 0014		00000028	6789+	LGF	R1, V3ADDR	load v3 source	
00008D02	E771 0000 0806		00000000	6790+	VL	v23, 0(R1)	use v22 to test decoder	
00008D08	E756 7010 1EFB			6791+	VCH	V21, V22, V23, 1, 1	test instruction	
00008D0E	B98D 0020			6792+	EPSW	R2, R0	extract psw	
00008D12	5020 500C		0000000C	6793+	ST	R2, CCPSW	to save CC	
00008D16	E750 5048 080E		00008CD0	6794+	VST	V21, V10159	save v1 output	
00008D1C	07FB			6795+	BR	R11	return	
00008D20				6796+RE159	DC	0F	V1 for this test	
00008D20				6797+	DROP	R5		
00008D20	FFFFFFFF FFFFFFFF			6798	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00008D28	FFFFFFFF	FFFFFFFF						
00008D30	01020304	05060708		6799	DC	XL16'	0102030405060708 090A0B0C0D0E0F10'	v2
00008D38	090A0B0C	0D0E0F10						
00008D40	00010203	04050607		6800	DC	XL16'	0001020304050607 08090A0B0C0D0E0F'	v3
00008D48	08090A0B	0C0D0E0F						
				6801				
				6802	VRR_B	VCH, 1, 0		
00008D50				6803+	DS	0FD		
00008D50		00008D50		6804+	USING	*, R5	base for test data and test routine	
00008D50	00008DB8			6805+T160	DC	A(X160)	address of test routine	
00008D54	00A0			6806+	DC	H' 160'	test number	
00008D56	00			6807+	DC	X' 00'		
00008D57	01			6808+	DC	HL1' 1'	m4 used	
00008D58	01			6809+	DC	HL1' 1'	m5 used	
00008D59	00			6810+	DC	HL1' 0'	CC	
00008D5A	07			6811+	DC	HL1' 7'	CC failed mask	
00008D5C	00000000	00000000		6812+	DS	2F	extracted PSW after test (has CC)	
00008D64	FF			6813+	DC	X' FF'	extracted CC, if test failed	
00008D65	E5C3C840	40404040		6814+	DC	CL8' VCH'	instruction name	
00008D70	00008DE8			6815+	DC	A(RE160)	address of v1 result	
00008D74	00008DF8			6816+	DC	A(RE160+16)	address of v2 source	
00008D78	00008E08			6817+	DC	A(RE160+32)	address of v3 source	
00008D7C	00000010			6818+	DC	A(16)	result length	
00008D80	00008DE8			6819+REA160	DC	A(RE160)	result address	
00008D88	00000000	00000000		6820+	DS	2FD	gap	
00008D90	00000000	00000000						
00008D98	00000000	00000000		6821+V10160	DS	XL16	V1 output	
00008DA0	00000000	00000000						
00008DA8	00000000	00000000		6822+	DS	2FD	gap	
00008DB0	00000000	00000000						
				6823+*				
00008DB8				6824+X160	DS	0F		
00008DB8	E310 5024 0014		00000024	6825+	LGF	R1, V2ADDR	load v2 source	
00008DBE	E761 0000 0806		00000000	6826+	VL	v22, 0(R1)	use v21 to test decoder	
00008DC4	E310 5028 0014		00000028	6827+	LGF	R1, V3ADDR	load v3 source	
00008DCA	E771 0000 0806		00000000	6828+	VL	v23, 0(R1)	use v22 to test decoder	
00008DD0	E756 7010 1EFB			6829+	VCH	V21, V22, V23, 1, 1	test instruction	
00008DD6	B98D 0020			6830+	EPSW	R2, R0	extract psw	
00008DDA	5020 500C		0000000C	6831+	ST	R2, CCPSW	to save CC	
00008DDE	E750 5048 080E		00008D98	6832+	VST	V21, V10160	save v1 output	
00008DE4	07FB			6833+	BR	R11	return	
00008DE8				6834+RE160	DC	0F	V1 for this test	
00008DE8				6835+	DROP	R5		
00008DE8	FFFFFFFF	FFFFFFFF		6836	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00008DF0	FFFFFFFF	FFFFFFFF						
00008DF8	00010203	04050607		6837	DC	XL16'	0001020304050607 08090A0B0C0D0E0F'	v2
00008E00	08090A0B	0C0D0E0F						
00008E08	FFFEFFFD	FFFCFFFB		6838	DC	XL16'	FFFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00008E10	FFFAFFF9	FFF8FFF7						
				6839				
				6840	VRR_B	VCH, 1, 1		
00008E18				6841+	DS	0FD		
00008E18		00008E18		6842+	USING	*, R5	base for test data and test routine	
00008E18	00008E80			6843+T161	DC	A(X161)	address of test routine	
00008E1C	00A1			6844+	DC	H' 161'	test number	
00008E1E	00			6845+	DC	X' 00'		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00008E1F	01			6846+	DC	HL1' 1' m4 used
00008E20	01			6847+	DC	HL1' 1' m5 used
00008E21	01			6848+	DC	HL1' 1' CC
00008E22	0B			6849+	DC	HL1' 11' CC failed mask
00008E24	00000000	00000000		6850+	DS	2F extracted PSW after test (has CC)
00008E2C	FF			6851+	DC	X' FF' extracted CC, if test failed
00008E2D	E5C3C840	40404040		6852+	DC	CL8' VCH' instruction name
00008E38	00008EB0			6853+	DC	A(RE161) address of v1 result
00008E3C	00008EC0			6854+	DC	A(RE161+16) address of v2 source
00008E40	00008ED0			6855+	DC	A(RE161+32) address of v3 source
00008E44	00000010			6856+	DC	A(16) result length
00008E48	00008EB0			6857+REA161	DC	A(RE161) result address
00008E50	00000000	00000000		6858+	DS	2FD gap
00008E58	00000000	00000000				
00008E60	00000000	00000000		6859+V10161	DS	XL16 V1 output
00008E68	00000000	00000000				
00008E70	00000000	00000000		6860+	DS	2FD gap
00008E78	00000000	00000000				
00008E80				6861+*		
00008E80	E310 5024 0014		00000024	6862+X161	DS	0F
00008E86	E761 0000 0806		00000000	6863+	LGF	R1, V2ADDR load v2 source
00008E8C	E310 5028 0014		00000028	6864+	VL	v22, 0(R1) use v21 to test decoder
00008E92	E771 0000 0806		00000000	6865+	LGF	R1, V3ADDR load v3 source
00008E98	E756 7010 1EFB			6866+	VL	v23, 0(R1) use v22 to test decoder
00008E9E	B98D 0020			6867+	VCH	V21, V22, V23, 1, 1 test instruction
00008EA2	5020 500C		0000000C	6868+	EPSW	R2, R0 extract psw
00008EA6	E750 5048 080E		00008E60	6869+	ST	R2, CCPSW to save CC
00008EAC	07FB			6870+	VST	V21, V10161 save v1 output
00008EB0				6871+	BR	R11 return
00008EB0				6872+RE161	DC	0F V1 for this test
00008EB0				6873+	DROP	R5
00008EB0	FFFF0000	0000FFFF		6874	DC	XL16' FFFF00000000FFFF 000000000000FFFF' result t
00008EB8	00000000	0000FFFF				
00008EC0	00110033	00550077		6875	DC	XL16' 0011003300550077 08090A0B0C0DFE1F' v2
00008EC8	08090A0B	0C0DFE1F				
00008ED0	00010203	04050067		6876	DC	XL16' 0001020304050067 08090A0B0C0DFE0F' v3
00008ED8	08090A0B	0C0DFE0F				
00008EE0				6877		
00008EE0				6878	VRR_B	VCH, 1, 1
00008EE0		00008EE0		6879+	DS	0FD
00008EE0	00008F48			6880+	USING	*, R5 base for test data and test routine
00008EE4	00A2			6881+T162	DC	A(X162) address of test routine
00008EE6	00			6882+	DC	H' 162' test number
00008EE7	01			6883+	DC	X' 00'
00008EE8	01			6884+	DC	HL1' 1' m4 used
00008EE9	01			6885+	DC	HL1' 1' m5 used
00008EEA	0B			6886+	DC	HL1' 1' CC
00008EEC	00000000	00000000		6887+	DC	HL1' 11' CC failed mask
00008EF4	FF			6888+	DS	2F extracted PSW after test (has CC)
00008EF5	E5C3C840	40404040		6889+	DC	X' FF' extracted CC, if test failed
00008F00	00008F78			6890+	DC	CL8' VCH' instruction name
00008F04	00008F88			6891+	DC	A(RE162) address of v1 result
00008F08	00008F98			6892+	DC	A(RE162+16) address of v2 source
00008F0C	00000010			6893+	DC	A(RE162+32) address of v3 source
00008F10	00008F78			6894+	DC	A(16) result length
				6895+REA162	DC	A(RE162) result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00008F18	00000000 00000000			6896+	DS	2FD	gap
00008F20	00000000 00000000						
00008F28	00000000 00000000			6897+V10162	DS	XL16	V1 output
00008F30	00000000 00000000						
00008F38	00000000 00000000			6898+	DS	2FD	gap
00008F40	00000000 00000000						
				6899+*			
00008F48				6900+X162	DS	0F	
00008F48	E310 5024 0014		00000024	6901+	LGF	R1, V2ADDR	load v2 source
00008F4E	E761 0000 0806		00000000	6902+	VL	v22, 0(R1)	use v21 to test decoder
00008F54	E310 5028 0014		00000028	6903+	LGF	R1, V3ADDR	load v3 source
00008F5A	E771 0000 0806		00000000	6904+	VL	v23, 0(R1)	use v22 to test decoder
00008F60	E756 7010 1EFB			6905+	VCH	V21, V22, V23, 1, 1	test instruction
00008F66	B98D 0020			6906+	EPSW	R2, R0	extract psw
00008F6A	5020 500C		0000000C	6907+	ST	R2, CCPSW	to save CC
00008F6E	E750 5048 080E		00008F28	6908+	VST	V21, V10162	save v1 output
00008F74	07FB			6909+	BR	R11	return
00008F78				6910+RE162	DC	0F	V1 for this test
00008F78				6911+	DROP	R5	
00008F78	00000000 0000FFFF			6912	DC	XL16' 000000000000FFFF FFFF00000000FFFF'	result t
00008F80	FFFF0000 0000FFFF						
00008F88	08090A0B 0C0DFE1F			6913	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
00008F90	00110033 00550077						
00008F98	08090A0B 0C0DFE0F			6914	DC	XL16' 08090A0B0C0DFE0F 0001020304050067'	v3
00008FA0	00010203 04050067						
				6915			
				6916	VRR_B	VCH, 1, 1	
00008FA8				6917+	DS	0FD	
00008FA8		00008FA8		6918+	USING	*, R5	base for test data and test routine
00008FA8	00009010			6919+T163	DC	A(X163)	address of test routine
00008FAC	00A3			6920+	DC	H' 163'	test number
00008FAE	00			6921+	DC	X' 00'	
00008FAF	01			6922+	DC	HL1' 1'	m4 used
00008FB0	01			6923+	DC	HL1' 1'	m5 used
00008FB1	01			6924+	DC	HL1' 1'	CC
00008FB2	0B			6925+	DC	HL1' 11'	CC failed mask
00008FB4	00000000 00000000			6926+	DS	2F	extracted PSW after test (has CC)
00008FBC	FF			6927+	DC	X' FF'	extracted CC, if test failed
00008FBD	E5C3C840 40404040			6928+	DC	CL8' VCH'	instruction name
00008FC8	00009040			6929+	DC	A(RE163)	address of v1 result
00008FCC	00009050			6930+	DC	A(RE163+16)	address of v2 source
00008FD0	00009060			6931+	DC	A(RE163+32)	address of v3 source
00008FD4	00000010			6932+	DC	A(16)	result length
00008FD8	00009040			6933+REA163	DC	A(RE163)	result address
00008FE0	00000000 00000000			6934+	DS	2FD	gap
00008FE8	00000000 00000000						
00008FF0	00000000 00000000			6935+V10163	DS	XL16	V1 output
00008FF8	00000000 00000000						
00009000	00000000 00000000			6936+	DS	2FD	gap
00009008	00000000 00000000						
				6937+*			
00009010				6938+X163	DS	0F	
00009010	E310 5024 0014		00000024	6939+	LGF	R1, V2ADDR	load v2 source
00009016	E761 0000 0806		00000000	6940+	VL	v22, 0(R1)	use v21 to test decoder
0000901C	E310 5028 0014		00000028	6941+	LGF	R1, V3ADDR	load v3 source
00009022	E771 0000 0806		00000000	6942+	VL	v23, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009028	E756 7010 1EFB			6943+	VCH	V21, V22, V23, 1, 1	test instruction
0000902E	B98D 0020			6944+	EPSW	R2, R0	extract psw
00009032	5020 500C		0000000C	6945+	ST	R2, CCPSW	to save CC
00009036	E750 5048 080E		00008FF0	6946+	VST	V21, V10163	save v1 output
0000903C	07FB			6947+	BR	R11	return
00009040				6948+RE163	DC	0F	V1 for this test
00009040				6949+	DROP	R5	
00009040	FFFFFFFF FFFFFFFF			6950	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result t
00009048	00000000 00000000						
00009050	00010203 04050607			6951	DC	XL16' 0001020304050607 FFFAFF9FFF8FFF7'	v2
00009058	FFFAFFF9 FFF8FFF7						
00009060	FFFEFFFD FFFCFFFB			6952	DC	XL16' FFFEFFFDFFFCFFFB 08090A0B0C0D0E0F'	v3
00009068	08090A0B 0C0D0E0F						
				6953			
00009070				6954	VRR_B	VCH, 1, 3	
00009070		00009070		6955+	DS	0FD	
00009070	000090D8			6956+	USING	*, R5	base for test data and test routine
00009074	00A4			6957+T164	DC	A(X164)	address of test routine
00009076	00			6958+	DC	H' 164'	test number
00009076	00			6959+	DC	X' 00'	
00009077	01			6960+	DC	HL1' 1'	m4 used
00009078	01			6961+	DC	HL1' 1'	m5 used
00009079	03			6962+	DC	HL1' 3'	CC
0000907A	0E			6963+	DC	HL1' 14'	CC failed mask
0000907C	00000000 00000000			6964+	DS	2F	extracted PSW after test (has CC)
00009084	FF			6965+	DC	X' FF'	extracted CC, if test failed
00009085	E5C3C840 40404040			6966+	DC	CL8' VCH'	instruction name
00009090	00009108			6967+	DC	A(RE164)	address of v1 result
00009094	00009118			6968+	DC	A(RE164+16)	address of v2 source
00009098	00009128			6969+	DC	A(RE164+32)	address of v3 source
0000909C	00000010			6970+	DC	A(16)	result length
000090A0	00009108			6971+REA164	DC	A(RE164)	result address
000090A8	00000000 00000000			6972+	DS	2FD	gap
000090B0	00000000 00000000						
000090B8	00000000 00000000			6973+V10164	DS	XL16	V1 output
000090C0	00000000 00000000						
000090C8	00000000 00000000			6974+	DS	2FD	gap
000090D0	00000000 00000000						
				6975+*			
000090D8				6976+X164	DS	0F	
000090D8	E310 5024 0014		00000024	6977+	LGF	R1, V2ADDR	load v2 source
000090DE	E761 0000 0806		00000000	6978+	VL	v22, 0(R1)	use v21 to test decoder
000090E4	E310 5028 0014		00000028	6979+	LGF	R1, V3ADDR	load v3 source
000090EA	E771 0000 0806		00000000	6980+	VL	v23, 0(R1)	use v22 to test decoder
000090F0	E756 7010 1EFB			6981+	VCH	V21, V22, V23, 1, 1	test instruction
000090F6	B98D 0020			6982+	EPSW	R2, R0	extract psw
000090FA	5020 500C		0000000C	6983+	ST	R2, CCPSW	to save CC
000090FE	E750 5048 080E		000090B8	6984+	VST	V21, V10164	save v1 output
00009104	07FB			6985+	BR	R11	return
00009108				6986+RE164	DC	0F	V1 for this test
00009108				6987+	DROP	R5	
00009108	00000000 00000000			6988	DC	XL16' 0000000000000000 0000000000000000'	result t
00009110	00000000 00000000						
00009118	00010003 04050607			6989	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00009120	00090A0B 0C0D0E0F						
00009128	01110233 11550677			6990	DC	XL16' 0111023311550677 1179116B514D312F'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00009130	1179116B 514D312F			6991				
00009138				6992	VRR_B	VCHL, 1, 3		
00009138		00009138		6993+	DS	0FD		
00009138	000091A0			6994+	USING	*, R5	base for test data and test routine	
0000913C	00A5			6995+T165	DC	A(X165)	address of test routine	
0000913E	00			6996+	DC	H' 165'	test number	
0000913F	01			6997+	DC	X' 00'		
00009140	01			6998+	DC	HL1' 1'	m4 used	
00009141	03			6999+	DC	HL1' 1'	m5 used	
00009142	0E			7000+	DC	HL1' 3'	CC	
00009144	00000000 00000000			7001+	DC	HL1' 14'	CC failed mask	
0000914C	FF			7002+	DS	2F	extracted PSW after test (has CC)	
0000914D	E5C3C8D3 40404040			7003+	DC	X' FF'	extracted CC, if test failed	
00009158	000091D0			7004+	DC	CL8' VCHL'	instruction name	
0000915C	000091E0			7005+	DC	A(RE165)	address of v1 result	
00009160	000091F0			7006+	DC	A(RE165+16)	address of v2 source	
00009164	00000010			7007+	DC	A(RE165+32)	address of v3 source	
00009168	000091D0			7008+	DC	A(16)	result length	
00009170	00000000 00000000			7009+REA165	DC	A(RE165)	result address	
00009178	00000000 00000000			7010+	DS	2FD	gap	
00009180	00000000 00000000			7011+V10165	DS	XL16	V1 output	
00009188	00000000 00000000							
00009190	00000000 00000000			7012+	DS	2FD	gap	
00009198	00000000 00000000							
000091A0				7013+*				
000091A0	E310 5024 0014		00000024	7014+X165	DS	0F		
000091A6	E761 0000 0806		00000000	7015+	LGF	R1, V2ADDR	load v2 source	
000091AC	E310 5028 0014		00000028	7016+	VL	v22, 0(R1)	use v21 to test decoder	
000091B2	E771 0000 0806		00000000	7017+	LGF	R1, V3ADDR	load v3 source	
000091B8	E756 7010 1EF9			7018+	VL	v23, 0(R1)	use v22 to test decoder	
000091BE	B98D 0020			7019+	VCHL	V21, V22, V23, 1, 1	test instruction	
000091C2	5020 500C		0000000C	7020+	EPSW	R2, R0	extract psw	
000091C6	E750 5048 080E		00009180	7021+	ST	R2, CCPSW	to save CC	
000091CC	07FB			7022+	VST	V21, V10165	save v1 output	
000091D0				7023+	BR	R11	return	
000091D0				7024+RE165	DC	0F	V1 for this test	
000091D0	00000000 00000000			7025+	DROP	R5		
000091D8	00000000 00000000			7026	DC	XL16' 0000000000000000 0000000000000000'	result t	
000091E0	08090A0B 0C0D0E0F			7027	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2	
000091E8	00010203 04050607							
000091F0	1179116B 514D312F			7028	DC	XL16' 1179116B514D312F 0111023311550677'	v3	
000091F8	01110233 11550677							
00009200				7029				
00009200		00009200		7030	VRR_B	VCH, 1, 3		
00009200	00009268			7031+	DS	0FD		
00009204	00A6			7032+	USING	*, R5	base for test data and test routine	
00009206	00			7033+T166	DC	A(X166)	address of test routine	
00009207	01			7034+	DC	H' 166'	test number	
00009208	01			7035+	DC	X' 00'		
00009209	03			7036+	DC	HL1' 1'	m4 used	
0000920A	0E			7037+	DC	HL1' 1'	m5 used	
				7038+	DC	HL1' 3'	CC	
				7039+	DC	HL1' 14'	CC failed mask	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000920C	00000000 00000000			7040+	DS	2F	extracted PSW after test (has CC)
00009214	FF			7041+	DC	X' FF'	extracted CC, if test failed
00009215	E5C3C840 40404040			7042+	DC	CL8' VCH'	instruction name
00009220	00009298			7043+	DC	A(RE166)	address of v1 result
00009224	000092A8			7044+	DC	A(RE166+16)	address of v2 source
00009228	000092B8			7045+	DC	A(RE166+32)	address of v3 source
0000922C	00000010			7046+	DC	A(16)	result length
00009230	00009298			7047+REA166	DC	A(RE166)	result address
00009238	00000000 00000000			7048+	DS	2FD	gap
00009240	00000000 00000000						
00009248	00000000 00000000			7049+V10166	DS	XL16	V1 output
00009250	00000000 00000000						
00009258	00000000 00000000			7050+	DS	2FD	gap
00009260	00000000 00000000						
00009268				7051+*			
00009268	E310 5024 0014		00000024	7052+X166	DS	0F	
0000926E	E761 0000 0806		00000000	7053+	LGF	R1, V2ADDR	load v2 source
00009274	E310 5028 0014		00000028	7054+	VL	v22, 0(R1)	use v21 to test decoder
0000927A	E771 0000 0806		00000000	7055+	LGF	R1, V3ADDR	load v3 source
00009280	E756 7010 1EFB			7056+	VL	v23, 0(R1)	use v22 to test decoder
00009286	B98D 0020			7057+	VCH	V21, V22, V23, 1, 1	test instruction
0000928A	5020 500C		0000000C	7058+	EPSW	R2, R0	extract psw
0000928E	E750 5048 080E		00009248	7059+	ST	R2, CCPSW	to save CC
00009294	07FB			7060+	VST	V21, V10166	save v1 output
00009298				7061+	BR	R11	return
00009298				7062+RE166	DC	0F	V1 for this test
00009298				7063+	DROP	R5	
00009298	00000000 00000000			7064	DC	XL16' 0000000000000000 0000000000000000'	result t
000092A0	00000000 00000000						
000092A8	FFFEFFFD FFFCFFFB			7065	DC	XL16' FFFEFFFDFFFCFFFB FFFAFFF9FFF8FFF7'	v2
000092B0	FFFAFFF9 FFF8FFF7						
000092B8	01110233 11550677			7066	DC	XL16' 0111023311550677 08090A0B0C0D0E0F'	v3
000092C0	08090A0B 0C0D0E0F						
				7067			
				7068 *Word			
000092C8				7069	VRR_B	VCH, 2, 0	
000092C8		000092C8		7070+	DS	0FD	
000092C8	00009330			7071+	USING	*, R5	base for test data and test routine
000092CC	00A7			7072+T167	DC	A(X167)	address of test routine
000092CE	00			7073+	DC	H' 167'	test number
000092CF	02			7074+	DC	X' 00'	
000092D0	01			7075+	DC	HL1' 2'	m4 used
000092D1	00			7076+	DC	HL1' 1'	m5 used
000092D2	07			7077+	DC	HL1' 0'	CC
000092D4	00000000 00000000			7078+	DC	HL1' 7'	CC failed mask
000092DC	FF			7079+	DS	2F	extracted PSW after test (has CC)
000092DD	E5C3C840 40404040			7080+	DC	X' FF'	extracted CC, if test failed
000092E8	00009360			7081+	DC	CL8' VCH'	instruction name
000092EC	00009370			7082+	DC	A(RE167)	address of v1 result
000092F0	00009380			7083+	DC	A(RE167+16)	address of v2 source
000092F4	00000010			7084+	DC	A(RE167+32)	address of v3 source
000092F8	00009360			7085+	DC	A(16)	result length
00009300	00000000 00000000			7086+REA167	DC	A(RE167)	result address
00009308	00000000 00000000			7087+	DS	2FD	gap
00009310	00000000 00000000			7088+V10167	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009318	00000000	00000000					
00009320	00000000	00000000		7089+	DS	2FD	gap
00009328	00000000	00000000					
00009330				7090+*			
00009330	E310 5024 0014		00000024	7091+X167	DS	0F	
00009336	E761 0000 0806		00000000	7092+	LGF	R1, V2ADDR	load v2 source
0000933C	E310 5028 0014		00000028	7093+	VL	v22, 0(R1)	use v21 to test decoder
00009342	E771 0000 0806		00000000	7094+	LGF	R1, V3ADDR	load v3 source
00009348	E756 7010 2EFB			7095+	VL	v23, 0(R1)	use v22 to test decoder
0000934E	B98D 0020			7096+	VCH	V21, V22, V23, 2, 1	test instruction
00009352	5020 500C		0000000C	7097+	EPSW	R2, R0	extract psw
00009356	E750 5048 080E		00009310	7098+	ST	R2, CCPSW	to save CC
0000935C	07FB			7099+	VST	V21, V10167	save v1 output
00009360				7100+	BR	R11	return
00009360				7101+RE167	DC	0F	V1 for this test
00009360	FFFFFFFF	FFFFFFFF		7102+	DROP	R5	
00009368	FFFFFFFF	FFFFFFFF		7103	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00009370	01020304 05060708			7104	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
00009378	090A0B0C 0D0E0F10						
00009380	00010203 04050607			7105	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
00009388	08090A0B 0C0D0E0F						
00009390				7106			
00009390			00009390	7107	VRR_B	VCH, 2, 0	
00009390	000093F8			7108+	DS	0FD	
00009394	00A8			7109+	USING	*, R5	base for test data and test routine
00009396	00			7110+T168	DC	A(X168)	address of test routine
00009397	02			7111+	DC	H' 168'	test number
00009398	01			7112+	DC	X' 00'	
00009399	00			7113+	DC	HL1' 2'	m4 used
0000939A	07			7114+	DC	HL1' 1'	m5 used
0000939C	00000000 00000000			7115+	DC	HL1' 0'	CC
000093A4	FF			7116+	DC	HL1' 7'	CC failed mask
000093A5	E5C3C840 40404040			7117+	DS	2F	extracted PSW after test (has CC)
000093B0	00009428			7118+	DC	X' FF'	extracted CC, if test failed
000093B4	00009438			7119+	DC	CL8' VCH'	instruction name
000093B8	00009448			7120+	DC	A(RE168)	address of v1 result
000093BC	00000010			7121+	DC	A(RE168+16)	address of v2 source
000093C0	00009428			7122+	DC	A(RE168+32)	address of v3 source
000093C8	00000000 00000000			7123+	DC	A(16)	result length
000093D0	00000000 00000000			7124+REA168	DC	A(RE168)	result address
000093D8	00000000 00000000			7125+	DS	2FD	gap
000093E0	00000000 00000000			7126+V10168	DS	XL16	V1 output
000093E8	00000000 00000000						
000093F0	00000000 00000000			7127+	DS	2FD	gap
000093F8				7128+*			
000093F8	E310 5024 0014		00000024	7129+X168	DS	0F	
000093FE	E761 0000 0806		00000000	7130+	LGF	R1, V2ADDR	load v2 source
00009404	E310 5028 0014		00000028	7131+	VL	v22, 0(R1)	use v21 to test decoder
0000940A	E771 0000 0806		00000000	7132+	LGF	R1, V3ADDR	load v3 source
00009410	E756 7010 2EFB			7133+	VL	v23, 0(R1)	use v22 to test decoder
00009416	B98D 0020			7134+	VCH	V21, V22, V23, 2, 1	test instruction
0000941A	5020 500C		0000000C	7135+	EPSW	R2, R0	extract psw
				7136+	ST	R2, CCPSW	to save CC

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
0000941E	E750 5048 080E		000093D8	7137+	VST	V21, V10168	save v1 output	
00009424	07FB			7138+	BR	R11	return	
00009428				7139+RE168	DC	0F	V1 for this test	
00009428				7140+	DROP	R5		
00009428	FFFFFFFF FFFFFFFF			7141	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t	
00009430	FFFFFFFF FFFFFFFF							
00009438	00010203 04050607			7142	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00009440	08090A0B 0C0D0E0F							
00009448	FFFEFFFD FFFCFFFB			7143	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3	
00009450	FFFAFF9 FFF8FFF7							
				7144				
00009458				7145	VRR_B	VCH, 2, 1		
00009458		00009458		7146+	DS	0FD		
00009458	000094C0			7147+	USING	*, R5	base for test data and test routine	
0000945C	00A9			7148+T169	DC	A(X169)	address of test routine	
0000945E	00			7149+	DC	H' 169'	test number	
0000945F	02			7150+	DC	X' 00'		
00009460	01			7151+	DC	HL1' 2'	m4 used	
00009461	01			7152+	DC	HL1' 1'	m5 used	
00009462	0B			7153+	DC	HL1' 1'	CC	
00009464	00000000 00000000			7154+	DC	HL1' 11'	CC failed mask	
0000946C	FF			7155+	DS	2F	extracted PSW after test (has CC)	
0000946D	E5C3C840 40404040			7156+	DC	X' FF'	extracted CC, if test failed	
00009478	000094F0			7157+	DC	CL8' VCH'	instruction name	
0000947C	00009500			7158+	DC	A(RE169)	address of v1 result	
00009480	00009510			7159+	DC	A(RE169+16)	address of v2 source	
00009484	00000010			7160+	DC	A(RE169+32)	address of v3 source	
00009488	000094F0			7161+	DC	A(16)	result length	
00009490	00000000 00000000			7162+REA169	DC	A(RE169)	result address	
00009498	00000000 00000000			7163+	DS	2FD	gap	
000094A0	00000000 00000000			7164+V10169	DS	XL16	V1 output	
000094A8	00000000 00000000							
000094B0	00000000 00000000			7165+	DS	2FD	gap	
000094B8	00000000 00000000							
				7166+*				
000094C0				7167+X169	DS	0F		
000094C0	E310 5024 0014		00000024	7168+	LGF	R1, V2ADDR	load v2 source	
000094C6	E761 0000 0806		00000000	7169+	VL	v22, 0(R1)	use v21 to test decoder	
000094CC	E310 5028 0014		00000028	7170+	LGF	R1, V3ADDR	load v3 source	
000094D2	E771 0000 0806		00000000	7171+	VL	v23, 0(R1)	use v22 to test decoder	
000094D8	E756 7010 2EFB			7172+	VCH	V21, V22, V23, 2, 1	test instruction	
000094DE	B98D 0020			7173+	EPSW	R2, R0	extract psw	
000094E2	5020 500C		0000000C	7174+	ST	R2, CCPSW	to save CC	
000094E6	E750 5048 080E		000094A0	7175+	VST	V21, V10169	save v1 output	
000094EC	07FB			7176+	BR	R11	return	
000094F0				7177+RE169	DC	0F	V1 for this test	
000094F0				7178+	DROP	R5		
000094F0	FFFFFFFF 00000000			7179	DC	XL16' FFFFFFFFF00000000 00000000FFFFFFFF'	result t	
000094F8	00000000 FFFFFFFF							
00009500	00110033 00550077			7180	DC	XL16' 0011003300550077 08090A0B0C0DFE1F'	v2	
00009508	08090A0B 0C0DFE1F							
00009510	00010203 04050067			7181	DC	XL16' 0001020304050067 08090A0B0C0DFE0F'	v3	
00009518	08090A0B 0C0DFE0F							
				7182				
				7183	VRR_B	VCH, 2, 1		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009520				7184+	DS	OFD	
00009520		00009520		7185+	USING	*, R5	base for test data and test routine
00009520	00009588			7186+T170	DC	A(X170)	address of test routine
00009524	00AA			7187+	DC	H' 170'	test number
00009526	00			7188+	DC	X' 00'	
00009527	02			7189+	DC	HL1' 2'	m4 used
00009528	01			7190+	DC	HL1' 1'	m5 used
00009529	01			7191+	DC	HL1' 1'	CC
0000952A	0B			7192+	DC	HL1' 11'	CC failed mask
0000952C	00000000 00000000			7193+	DS	2F	extracted PSW after test (has CC)
00009534	FF			7194+	DC	X' FF'	extracted CC, if test failed
00009535	E5C3C840 40404040			7195+	DC	CL8' VCH'	instruction name
00009540	000095B8			7196+	DC	A(RE170)	address of v1 result
00009544	000095C8			7197+	DC	A(RE170+16)	address of v2 source
00009548	000095D8			7198+	DC	A(RE170+32)	address of v3 source
0000954C	00000010			7199+	DC	A(16)	result length
00009550	000095B8			7200+REA170	DC	A(RE170)	result address
00009558	00000000 00000000			7201+	DS	2FD	gap
00009560	00000000 00000000						
00009568	00000000 00000000			7202+V10170	DS	XL16	V1 output
00009570	00000000 00000000						
00009578	00000000 00000000			7203+	DS	2FD	gap
00009580	00000000 00000000						
00009588				7204+*			
00009588	E310 5024 0014		00000024	7205+X170	DS	OF	
0000958E	E761 0000 0806		00000000	7206+	LGF	R1, V2ADDR	load v2 source
00009594	E310 5028 0014		00000028	7207+	VL	v22, 0(R1)	use v21 to test decoder
0000959A	E771 0000 0806		00000000	7208+	LGF	R1, V3ADDR	load v3 source
000095A0	E756 7010 2EFB			7209+	VL	v23, 0(R1)	use v22 to test decoder
000095A6	B98D 0020			7210+	VCH	V21, V22, V23, 2, 1	test instruction
000095AA	5020 500C		0000000C	7211+	EPSW	R2, R0	extract psw
000095AE	E750 5048 080E		00009568	7212+	ST	R2, CCPSW	to save CC
000095B4	07FB			7213+	VST	V21, V10170	save v1 output
000095B8				7214+	BR	R11	return
000095B8				7215+RE170	DC	OF	V1 for this test
000095B8				7216+	DROP	R5	
000095B8	00000000 FFFFFFFF			7217	DC	XL16' 00000000FFFFFFFF FFFFFFFF00000000'	result
000095C0	FFFFFFFF 00000000						
000095C8	08090A0B 0C0DFE1F			7218	DC	XL16' 08090A0B0C0DFE1F 0011003300550077'	v2
000095D0	00110033 00550077						
000095D8	08090A0B 0C0DFE0F			7219	DC	XL16' 08090A0B0C0DFE0F 0001020304050067'	v3
000095E0	00010203 04050067						
000095E8				7220			
000095E8		000095E8		7221	VRR_B	VCH, 2, 1	
000095E8	00009650			7222+	DS	OFD	
000095EC	00AB			7223+	USING	*, R5	base for test data and test routine
000095EE	00			7224+T171	DC	A(X171)	address of test routine
000095EF	02			7225+	DC	H' 171'	test number
000095F0	01			7226+	DC	X' 00'	
000095F1	01			7227+	DC	HL1' 2'	m4 used
000095F2	0B			7228+	DC	HL1' 1'	m5 used
000095F4	00000000 00000000			7229+	DC	HL1' 1'	CC
000095FC	FF			7230+	DC	HL1' 11'	CC failed mask
000095FD	E5C3C840 40404040			7231+	DS	2F	extracted PSW after test (has CC)
				7232+	DC	X' FF'	extracted CC, if test failed
				7233+	DC	CL8' VCH'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009608	00009680			7234+	DC	A(RE171)	address of v1 result
0000960C	00009690			7235+	DC	A(RE171+16)	address of v2 source
00009610	000096A0			7236+	DC	A(RE171+32)	address of v3 source
00009614	00000010			7237+	DC	A(16)	result length
00009618	00009680			7238+REA171	DC	A(RE171)	result address
00009620	00000000 00000000			7239+	DS	2FD	gap
00009628	00000000 00000000						
00009630	00000000 00000000			7240+V10171	DS	XL16	V1 output
00009638	00000000 00000000						
00009640	00000000 00000000			7241+	DS	2FD	gap
00009648	00000000 00000000						
00009650				7242+*			
00009650	E310 5024 0014		00000024	7243+X171	DS	0F	
00009656	E761 0000 0806		00000000	7244+	LGF	R1, V2ADDR	load v2 source
0000965C	E310 5028 0014		00000028	7245+	VL	v22, 0(R1)	use v21 to test decoder
00009662	E771 0000 0806		00000000	7246+	LGF	R1, V3ADDR	load v3 source
00009668	E756 7010 2EFB			7247+	VL	v23, 0(R1)	use v22 to test decoder
0000966E	B98D 0020			7248+	VCH	V21, V22, V23, 2, 1	test instruction
00009672	5020 500C		0000000C	7249+	EPSW	R2, R0	extract psw
00009676	E750 5048 080E		00009630	7250+	ST	R2, CCPSW	to save CC
0000967C	07FB			7251+	VST	V21, V10171	save v1 output
00009680				7252+	BR	R11	return
00009680				7253+RE171	DC	0F	V1 for this test
00009680	FFFFFFFF FFFFFFFF			7254+	DROP	R5	
00009688	00000000 00000000			7255	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result
00009690	00010203 04050607			7256	DC	XL16' 0001020304050607 FFFAFF9FFF8FFF7'	v2
00009698	FFFAFFF9 FFF8FFF7						
000096A0	FFFEFFFD FFFCFFFB			7257	DC	XL16' FFFEFFDFFFCFFFB 08090A0B0C0D0E0F'	v3
000096A8	08090A0B 0C0D0E0F						
000096B0				7258			
000096B0				7259	VRR_B	VCH, 2, 3	
000096B0	00009718	000096B0		7260+	DS	0FD	
000096B4	00AC			7261+	USING	*, R5	base for test data and test routine
000096B6	00			7262+T172	DC	A(X172)	address of test routine
000096B7	02			7263+	DC	H' 172'	test number
000096B8	01			7264+	DC	X' 00'	
000096B9	03			7265+	DC	HL1' 2'	m4 used
000096BA	0E			7266+	DC	HL1' 1'	m5 used
000096BC	00000000 00000000			7267+	DC	HL1' 3'	CC
000096C4	FF			7268+	DC	HL1' 14'	CC failed mask
000096C5	E5C3C840 40404040			7269+	DS	2F	extracted PSW after test (has CC)
000096D0	00009748			7270+	DC	X' FF'	extracted CC, if test failed
000096D4	00009758			7271+	DC	CL8' VCH'	instruction name
000096D8	00009768			7272+	DC	A(RE172)	address of v1 result
000096DC	00000010			7273+	DC	A(RE172+16)	address of v2 source
000096E0	00009748			7274+	DC	A(RE172+32)	address of v3 source
000096E8	00000000 00000000			7275+	DC	A(16)	result length
000096F0	00000000 00000000			7276+REA172	DC	A(RE172)	result address
000096F8	00000000 00000000			7277+	DS	2FD	gap
00009700	00000000 00000000						
00009708	00000000 00000000			7278+V10172	DS	XL16	V1 output
00009710	00000000 00000000			7279+	DS	2FD	gap
				7280+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009718				7281+X172	DS	0F	
00009718	E310 5024 0014		00000024	7282+	LGF	R1, V2ADDR	load v2 source
0000971E	E761 0000 0806		00000000	7283+	VL	v22, 0(R1)	use v21 to test decoder
00009724	E310 5028 0014		00000028	7284+	LGF	R1, V3ADDR	load v3 source
0000972A	E771 0000 0806		00000000	7285+	VL	v23, 0(R1)	use v22 to test decoder
00009730	E756 7010 2EFB			7286+	VCH	V21, V22, V23, 2, 1	test instruction
00009736	B98D 0020			7287+	EPSW	R2, R0	extract psw
0000973A	5020 500C		0000000C	7288+	ST	R2, CCPSW	to save CC
0000973E	E750 5048 080E		000096F8	7289+	VST	V21, V10172	save v1 output
00009744	07FB			7290+	BR	R11	return
00009748				7291+RE172	DC	0F	V1 for this test
00009748				7292+	DROP	R5	
00009748	00000000 00000000			7293	DC	XL16' 0000000000000000 0000000000000000'	result
00009750	00000000 00000000						
00009758	00010003 04050607			7294	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00009760	00090A0B 0C0D0E0F						
00009768	01110233 11550677			7295	DC	XL16' 0111023311550677 1179116B514D312F'	v3
00009770	1179116B 514D312F						
				7296			
				7297	VRR_B	VCHL, 2, 3	
00009778				7298+	DS	0FD	
00009778		00009778		7299+	USING	*, R5	base for test data and test routine
00009778	000097E0			7300+T173	DC	A(X173)	address of test routine
0000977C	00AD			7301+	DC	H' 173'	test number
0000977E	00			7302+	DC	X' 00'	
0000977F	02			7303+	DC	HL1' 2'	m4 used
00009780	01			7304+	DC	HL1' 1'	m5 used
00009781	03			7305+	DC	HL1' 3'	CC
00009782	0E			7306+	DC	HL1' 14'	CC failed mask
00009784	00000000 00000000			7307+	DS	2F	extracted PSW after test (has CC)
0000978C	FF			7308+	DC	X' FF'	extracted CC, if test failed
0000978D	E5C3C8D3 40404040			7309+	DC	CL8' VCHL'	instruction name
00009798	00009810			7310+	DC	A(RE173)	address of v1 result
0000979C	00009820			7311+	DC	A(RE173+16)	address of v2 source
000097A0	00009830			7312+	DC	A(RE173+32)	address of v3 source
000097A4	00000010			7313+	DC	A(16)	result length
000097A8	00009810			7314+REA173	DC	A(RE173)	result address
000097B0	00000000 00000000			7315+	DS	2FD	gap
000097B8	00000000 00000000						
000097C0	00000000 00000000			7316+V10173	DS	XL16	V1 output
000097C8	00000000 00000000						
000097D0	00000000 00000000			7317+	DS	2FD	gap
000097D8	00000000 00000000						
				7318+*			
000097E0				7319+X173	DS	0F	
000097E0	E310 5024 0014		00000024	7320+	LGF	R1, V2ADDR	load v2 source
000097E6	E761 0000 0806		00000000	7321+	VL	v22, 0(R1)	use v21 to test decoder
000097EC	E310 5028 0014		00000028	7322+	LGF	R1, V3ADDR	load v3 source
000097F2	E771 0000 0806		00000000	7323+	VL	v23, 0(R1)	use v22 to test decoder
000097F8	E756 7010 2EF9			7324+	VCHL	V21, V22, V23, 2, 1	test instruction
000097FE	B98D 0020			7325+	EPSW	R2, R0	extract psw
00009802	5020 500C		0000000C	7326+	ST	R2, CCPSW	to save CC
00009806	E750 5048 080E		000097C0	7327+	VST	V21, V10173	save v1 output
0000980C	07FB			7328+	BR	R11	return
00009810				7329+RE173	DC	0F	V1 for this test
00009810				7330+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009810	00000000 00000000			7331	DC	XL16' 0000000000000000 0000000000000000'	result
00009818	00000000 00000000						
00009820	08090A0B 0C0D0E0F			7332	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00009828	00010203 04050607						
00009830	1179116B 514D312F			7333	DC	XL16' 1179116B514D312F 0111023311550677'	v3
00009838	01110233 11550677						
				7334			
				7335	VRR_B	VCH, 2, 3	
00009840				7336+	DS	0FD	
00009840		00009840		7337+	USING	*, R5	base for test data and test routine
00009840	000098A8			7338+T174	DC	A(X174)	address of test routine
00009844	00AE			7339+	DC	H' 174'	test number
00009846	00			7340+	DC	X' 00'	
00009847	02			7341+	DC	HL1' 2'	m4 used
00009848	01			7342+	DC	HL1' 1'	m5 used
00009849	03			7343+	DC	HL1' 3'	CC
0000984A	0E			7344+	DC	HL1' 14'	CC failed mask
0000984C	00000000 00000000			7345+	DS	2F	extracted PSW after test (has CC)
00009854	FF			7346+	DC	X' FF'	extracted CC, if test failed
00009855	E5C3C840 40404040			7347+	DC	CL8' VCH'	instruction name
00009860	000098D8			7348+	DC	A(RE174)	address of v1 result
00009864	000098E8			7349+	DC	A(RE174+16)	address of v2 source
00009868	000098F8			7350+	DC	A(RE174+32)	address of v3 source
0000986C	00000010			7351+	DC	A(16)	result length
00009870	000098D8			7352+REA174	DC	A(RE174)	result address
00009878	00000000 00000000			7353+	DS	2FD	gap
00009880	00000000 00000000						
00009888	00000000 00000000			7354+V10174	DS	XL16	V1 output
00009890	00000000 00000000						
00009898	00000000 00000000			7355+	DS	2FD	gap
000098A0	00000000 00000000						
				7356+*			
000098A8				7357+X174	DS	0F	
000098A8	E310 5024 0014		00000024	7358+	LGF	R1, V2ADDR	load v2 source
000098AE	E761 0000 0806		00000000	7359+	VL	v22, 0(R1)	use v21 to test decoder
000098B4	E310 5028 0014		00000028	7360+	LGF	R1, V3ADDR	load v3 source
000098BA	E771 0000 0806		00000000	7361+	VL	v23, 0(R1)	use v22 to test decoder
000098C0	E756 7010 2EFB			7362+	VCH	V21, V22, V23, 2, 1	test instruction
000098C6	B98D 0020			7363+	EPSW	R2, R0	extract psw
000098CA	5020 500C		0000000C	7364+	ST	R2, CCPSW	to save CC
000098CE	E750 5048 080E		00009888	7365+	VST	V21, V10174	save v1 output
000098D4	07FB			7366+	BR	R11	return
000098D8				7367+RE174	DC	0F	V1 for this test
000098D8				7368+	DROP	R5	
000098D8	00000000 00000000			7369	DC	XL16' 0000000000000000 0000000000000000'	result
000098E0	00000000 00000000						
000098E8	FFFEFFFD FFFCFFFB			7370	DC	XL16' FFFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v2
000098F0	FFFAFFF9 FFF8FFF7						
000098F8	01110233 11550677			7371	DC	XL16' 0111023311550677 08090A0B0C0D0E0F'	v3
00009900	08090A0B 0C0D0E0F						
				7372			
				7373	*Doubleword		
				7374	VRR_B	VCH, 3, 0	
00009908				7375+	DS	0FD	
00009908		00009908		7376+	USING	*, R5	base for test data and test routine
00009908	00009970			7377+T175	DC	A(X175)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000990C	00AF			7378+	DC	H' 175'	test number
0000990E	00			7379+	DC	X' 00'	
0000990F	03			7380+	DC	HL1' 3'	m4 used
00009910	01			7381+	DC	HL1' 1'	m5 used
00009911	00			7382+	DC	HL1' 0'	CC
00009912	07			7383+	DC	HL1' 7'	CC failed mask
00009914	00000000 00000000			7384+	DS	2F	extracted PSW after test (has CC)
0000991C	FF			7385+	DC	X' FF'	extracted CC, if test failed
0000991D	E5C3C840 40404040			7386+	DC	CL8' VCH'	instruction name
00009928	000099A0			7387+	DC	A(RE175)	address of v1 result
0000992C	000099B0			7388+	DC	A(RE175+16)	address of v2 source
00009930	000099C0			7389+	DC	A(RE175+32)	address of v3 source
00009934	00000010			7390+	DC	A(16)	result length
00009938	000099A0			7391+REA175	DC	A(RE175)	result address
00009940	00000000 00000000			7392+	DS	2FD	gap
00009948	00000000 00000000						
00009950	00000000 00000000			7393+V10175	DS	XL16	V1 output
00009958	00000000 00000000						
00009960	00000000 00000000			7394+	DS	2FD	gap
00009968	00000000 00000000						
00009970				7395+*			
00009970	E310 5024 0014		00000024	7396+X175	DS	0F	
00009976	E761 0000 0806		00000000	7397+	LGF	R1, V2ADDR	load v2 source
0000997C	E310 5028 0014		00000028	7398+	VL	v22, 0(R1)	use v21 to test decoder
00009982	E771 0000 0806		00000000	7399+	LGF	R1, V3ADDR	load v3 source
00009988	E756 7010 3EFB		00000000	7400+	VL	v23, 0(R1)	use v22 to test decoder
00009988	E756 7010 3EFB			7401+	VCH	V21, V22, V23, 3, 1	test instruction
0000998E	B98D 0020			7402+	EPSW	R2, R0	extract psw
00009992	5020 500C		0000000C	7403+	ST	R2, CCPSW	to save CC
00009996	E750 5048 080E		00009950	7404+	VST	V21, V10175	save v1 output
0000999C	07FB			7405+	BR	R11	return
000099A0				7406+RE175	DC	0F	V1 for this test
000099A0				7407+	DROP	R5	
000099A0	FFFFFFFF FFFFFFFF			7408	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000099A8	FFFFFFFF FFFFFFFF						
000099B0	01020304 05060708			7409	DC	XL16' 0102030405060708 090A0B0C0D0E0F10'	v2
000099B8	090A0B0C 0D0E0F10						
000099C0	00010203 04050607			7410	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3
000099C8	08090A0B 0C0D0E0F						
000099D0				7411			
000099D0				7412	VRR_B	VCH, 3, 0	
000099D0		000099D0		7413+	DS	0FD	
000099D0	00009A38			7414+	USING	*, R5	base for test data and test routine
000099D4	00B0			7415+T176	DC	A(X176)	address of test routine
000099D6	00			7416+	DC	H' 176'	test number
000099D6	00			7417+	DC	X' 00'	
000099D7	03			7418+	DC	HL1' 3'	m4 used
000099D8	01			7419+	DC	HL1' 1'	m5 used
000099D9	00			7420+	DC	HL1' 0'	CC
000099DA	07			7421+	DC	HL1' 7'	CC failed mask
000099DC	00000000 00000000			7422+	DS	2F	extracted PSW after test (has CC)
000099E4	FF			7423+	DC	X' FF'	extracted CC, if test failed
000099E5	E5C3C840 40404040			7424+	DC	CL8' VCH'	instruction name
000099F0	00009A68			7425+	DC	A(RE176)	address of v1 result
000099F4	00009A78			7426+	DC	A(RE176+16)	address of v2 source
000099F8	00009A88			7427+	DC	A(RE176+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000099FC	00000010			7428+	DC	A(16)	result length
00009A00	00009A68			7429+REA176	DC	A(RE176)	result address
00009A08	00000000 00000000			7430+	DS	2FD	gap
00009A10	00000000 00000000						
00009A18	00000000 00000000			7431+V10176	DS	XL16	V1 output
00009A20	00000000 00000000						
00009A28	00000000 00000000			7432+	DS	2FD	gap
00009A30	00000000 00000000						
00009A38				7433+*			
00009A38	E310 5024 0014		00000024	7434+X176	DS	0F	
00009A3E	E761 0000 0806		00000000	7435+	LGF	R1, V2ADDR	load v2 source
00009A44	E310 5028 0014		00000028	7436+	VL	v22, 0(R1)	use v21 to test decoder
00009A4A	E771 0000 0806		00000000	7437+	LGF	R1, V3ADDR	load v3 source
00009A50	E756 7010 3EFB			7438+	VL	v23, 0(R1)	use v22 to test decoder
00009A56	B98D 0020			7439+	VCH	V21, V22, V23, 3, 1	test instruction
00009A5A	5020 500C		0000000C	7440+	EPSW	R2, R0	extract psw
00009A5E	E750 5048 080E		00009A18	7441+	ST	R2, CCPSW	to save CC
00009A64	07FB			7442+	VST	V21, V10176	save v1 output
00009A68				7443+	BR	R11	return
00009A68				7444+RE176	DC	0F	V1 for this test
00009A68	FFFFFFFF FFFFFFFF			7445+	DROP	R5	
00009A70	FFFFFFFF FFFFFFFF			7446	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00009A78	00010203 04050607			7447	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00009A80	08090A0B 0C0D0E0F						
00009A88	FFFEFFFD FFFCFFFB			7448	DC	XL16' FFEFFFDFFFCFFFB FFFAFF9FFF8FFF7'	v3
00009A90	FFFAFF9 FFF8FFF7						
00009A98				7449			
00009A98		00009A98		7450	VRR_B	VCH, 3, 1	
00009A98	00009B00			7451+	DS	0FD	
00009A9C	00B1			7452+	USING	*, R5	base for test data and test routine
00009A9E	00			7453+T177	DC	A(X177)	address of test routine
00009A9F	03			7454+	DC	H' 177'	test number
00009AA0	01			7455+	DC	X' 00'	
00009AA1	01			7456+	DC	HL1' 3'	m4 used
00009AA2	0B			7457+	DC	HL1' 1'	m5 used
00009AA4	00000000 00000000			7458+	DC	HL1' 1'	CC
00009AAC	FF			7459+	DC	HL1' 11'	CC failed mask
00009AAD	E5C3C840 40404040			7460+	DS	2F	extracted PSW after test (has CC)
00009AB8	00009B30			7461+	DC	X' FF'	extracted CC, if test failed
00009ABC	00009B40			7462+	DC	CL8' VCH'	instruction name
00009AC0	00009B50			7463+	DC	A(RE177)	address of v1 result
00009AC4	00000010			7464+	DC	A(RE177+16)	address of v2 source
00009AC8	00009B30			7465+	DC	A(RE177+32)	address of v3 source
00009AD0	00000000 00000000			7466+	DC	A(16)	result length
00009AD8	00000000 00000000			7467+REA177	DC	A(RE177)	result address
00009AE0	00000000 00000000			7468+	DS	2FD	gap
00009AE8	00000000 00000000						
00009AF0	00000000 00000000			7469+V10177	DS	XL16	V1 output
00009AF8	00000000 00000000			7470+	DS	2FD	gap
00009B00				7471+*			
00009B00	E310 5024 0014		00000024	7472+X177	DS	0F	
00009B06	E761 0000 0806		00000000	7473+	LGF	R1, V2ADDR	load v2 source
				7474+	VL	v22, 0(R1)	use v21 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00009B0C	E310 5028 0014		00000028	7475+	LGF	R1, V3ADDR	load v3 source	
00009B12	E771 0000 0806		00000000	7476+	VL	v23, 0(R1)	use v22 to test decoder	
00009B18	E756 7010 3EFB			7477+	VCH	V21, V22, V23, 3, 1	test instruction	
00009B1E	B98D 0020			7478+	EPSW	R2, R0	extract psw	
00009B22	5020 500C		0000000C	7479+	ST	R2, CCPSW	to save CC	
00009B26	E750 5048 080E		00009AE0	7480+	VST	V21, V10177	save v1 output	
00009B2C	07FB			7481+	BR	R11	return	
00009B30				7482+RE177	DC	0F	V1 for this test	
00009B30				7483+	DROP	R5		
00009B30	FFFFFFFF FFFFFFFF			7484	DC	XL16' FFFFFFFFFFFFFFFFFF 0000000000000000'	result t	
00009B38	00000000 00000000							
00009B40	00110033 00550077			7485	DC	XL16' 0011003300550077 08090A0B0C0DFE0F'	v2	
00009B48	08090A0B 0C0DFE0F							
00009B50	00010203 04050067			7486	DC	XL16' 0001020304050067 08090A0B0C0DFE1F'	v3	
00009B58	08090A0B 0C0DFE1F							
				7487				
				7488	VRR_B	VCH, 3, 1		
00009B60				7489+	DS	0FD		
00009B60		00009B60		7490+	USING	*, R5	base for test data and test routine	
00009B60	00009BC8			7491+T178	DC	A(X178)	address of test routine	
00009B64	00B2			7492+	DC	H' 178'	test number	
00009B66	00			7493+	DC	X' 00'		
00009B67	03			7494+	DC	HL1' 3'	m4 used	
00009B68	01			7495+	DC	HL1' 1'	m5 used	
00009B69	01			7496+	DC	HL1' 1'	CC	
00009B6A	0B			7497+	DC	HL1' 11'	CC failed mask	
00009B6C	00000000 00000000			7498+	DS	2F	extracted PSW after test (has CC)	
00009B74	FF			7499+	DC	X' FF'	extracted CC, if test failed	
00009B75	E5C3C840 40404040			7500+	DC	CL8' VCH'	instruction name	
00009B80	00009BF8			7501+	DC	A(RE178)	address of v1 result	
00009B84	00009C08			7502+	DC	A(RE178+16)	address of v2 source	
00009B88	00009C18			7503+	DC	A(RE178+32)	address of v3 source	
00009B8C	00000010			7504+	DC	A(16)	result length	
00009B90	00009BF8			7505+REA178	DC	A(RE178)	result address	
00009B98	00000000 00000000			7506+	DS	2FD	gap	
00009BA0	00000000 00000000							
00009BA8	00000000 00000000			7507+V10178	DS	XL16	V1 output	
00009BB0	00000000 00000000							
00009BB8	00000000 00000000			7508+	DS	2FD	gap	
00009BC0	00000000 00000000							
				7509+*				
00009BC8				7510+X178	DS	0F		
00009BC8	E310 5024 0014		00000024	7511+	LGF	R1, V2ADDR	load v2 source	
00009BCE	E761 0000 0806		00000000	7512+	VL	v22, 0(R1)	use v21 to test decoder	
00009BD4	E310 5028 0014		00000028	7513+	LGF	R1, V3ADDR	load v3 source	
00009BDA	E771 0000 0806		00000000	7514+	VL	v23, 0(R1)	use v22 to test decoder	
00009BE0	E756 7010 3EFB			7515+	VCH	V21, V22, V23, 3, 1	test instruction	
00009BE6	B98D 0020			7516+	EPSW	R2, R0	extract psw	
00009BEA	5020 500C		0000000C	7517+	ST	R2, CCPSW	to save CC	
00009BEE	E750 5048 080E		00009BA8	7518+	VST	V21, V10178	save v1 output	
00009BF4	07FB			7519+	BR	R11	return	
00009BF8				7520+RE178	DC	0F	V1 for this test	
00009BF8				7521+	DROP	R5		
00009BF8	00000000 00000000			7522	DC	XL16' 0000000000000000 FFFFFFFFFFFFFFFFFF'	result t	
00009C00	FFFFFFFF FFFFFFFF							
00009C08	08090A0B 0C0DFE0F			7523	DC	XL16' 08090A0B0C0DFE0F 0011003300550077'	v2	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00009C10	00110033 00550077							
00009C18	08090A0B 0C0DFE1F			7524	DC	XL16' 08090A0B0C0DFE1F	0001020304050067'	v3
00009C20	00010203 04050067							
				7525				
				7526	VRR_B	VCH, 3, 1		
00009C28				7527+	DS	0FD		
00009C28		00009C28		7528+	USING	*, R5		base for test data and test routine
00009C28	00009C90			7529+T179	DC	A(X179)		address of test routine
00009C2C	00B3			7530+	DC	H' 179'		test number
00009C2E	00			7531+	DC	X' 00'		
00009C2F	03			7532+	DC	HL1' 3'	m4 used	
00009C30	01			7533+	DC	HL1' 1'	m5 used	
00009C31	01			7534+	DC	HL1' 1'	CC	
00009C32	0B			7535+	DC	HL1' 11'	CC failed mask	
00009C34	00000000 00000000			7536+	DS	2F	extracted PSW after test (has CC)	
00009C3C	FF			7537+	DC	X' FF'	extracted CC, if test failed	
00009C3D	E5C3C840 40404040			7538+	DC	CL8' VCH'	instruction name	
00009C48	00009CC0			7539+	DC	A(RE179)	address of v1 result	
00009C4C	00009CD0			7540+	DC	A(RE179+16)	address of v2 source	
00009C50	00009CE0			7541+	DC	A(RE179+32)	address of v3 source	
00009C54	00000010			7542+	DC	A(16)	result length	
00009C58	00009CC0			7543+REA179	DC	A(RE179)	result address	
00009C60	00000000 00000000			7544+	DS	2FD	gap	
00009C68	00000000 00000000							
00009C70	00000000 00000000			7545+V10179	DS	XL16	V1 output	
00009C78	00000000 00000000							
00009C80	00000000 00000000			7546+	DS	2FD	gap	
00009C88	00000000 00000000							
				7547+*				
00009C90				7548+X179	DS	0F		
00009C90	E310 5024 0014		00000024	7549+	LGF	R1, V2ADDR	load v2 source	
00009C96	E761 0000 0806		00000000	7550+	VL	v22, 0(R1)	use v21 to test decoder	
00009C9C	E310 5028 0014		00000028	7551+	LGF	R1, V3ADDR	load v3 source	
00009CA2	E771 0000 0806		00000000	7552+	VL	v23, 0(R1)	use v22 to test decoder	
00009CA8	E756 7010 3EFB			7553+	VCH	V21, V22, V23, 3, 1	test instruction	
00009CAE	B98D 0020			7554+	EPSW	R2, R0	extract psw	
00009CB2	5020 500C		0000000C	7555+	ST	R2, CCPSW	to save CC	
00009CB6	E750 5048 080E		00009C70	7556+	VST	V21, V10179	save v1 output	
00009CBC	07FB			7557+	BR	R11	return	
00009CC0				7558+RE179	DC	0F	V1 for this test	
00009CC0				7559+	DROP	R5		
00009CC0	FFFFFFFF FFFFFFFF			7560	DC	XL16' FFFFFFFFFFFFFFFFFF	0000000000000000'	result t
00009CC8	00000000 00000000							
00009CD0	00010203 04050607			7561	DC	XL16' 0001020304050607	FFFAFFF9FFF8FFF7'	v2
00009CD8	FFFAFFF9 FFF8FFF7							
00009CE0	FFFEFFFD FFFCFFFB			7562	DC	XL16' FFFEFFFDFFFCFFFB	08090A0B0C0D0E0F'	v3
00009CE8	08090A0B 0C0D0E0F							
				7563				
				7564	VRR_B	VCH, 3, 3		
00009CF0				7565+	DS	0FD		
00009CF0		00009CF0		7566+	USING	*, R5		base for test data and test routine
00009CF0	00009D58			7567+T180	DC	A(X180)		address of test routine
00009CF4	00B4			7568+	DC	H' 180'		test number
00009CF6	00			7569+	DC	X' 00'		
00009CF7	03			7570+	DC	HL1' 3'	m4 used	
00009CF8	01			7571+	DC	HL1' 1'	m5 used	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009CF9	03			7572+	DC	HL1' 3'	CC
00009CFA	0E			7573+	DC	HL1' 14'	CC failed mask
00009CFC	00000000	00000000		7574+	DS	2F	extracted PSW after test (has CC)
00009D04	FF			7575+	DC	X' FF'	extracted CC, if test failed
00009D05	E5C3C840	40404040		7576+	DC	CL8' VCH'	instruction name
00009D10	00009D88			7577+	DC	A(RE180)	address of v1 result
00009D14	00009D98			7578+	DC	A(RE180+16)	address of v2 source
00009D18	00009DA8			7579+	DC	A(RE180+32)	address of v3 source
00009D1C	00000010			7580+	DC	A(16)	result length
00009D20	00009D88			7581+REA180	DC	A(RE180)	result address
00009D28	00000000	00000000		7582+	DS	2FD	gap
00009D30	00000000	00000000					
00009D38	00000000	00000000		7583+V10180	DS	XL16	V1 output
00009D40	00000000	00000000					
00009D48	00000000	00000000		7584+	DS	2FD	gap
00009D50	00000000	00000000					
				7585+*			
00009D58				7586+X180	DS	0F	
00009D58	E310 5024 0014		00000024	7587+	LGF	R1, V2ADDR	load v2 source
00009D5E	E761 0000 0806		00000000	7588+	VL	v22, 0(R1)	use v21 to test decoder
00009D64	E310 5028 0014		00000028	7589+	LGF	R1, V3ADDR	load v3 source
00009D6A	E771 0000 0806		00000000	7590+	VL	v23, 0(R1)	use v22 to test decoder
00009D70	E756 7010 3EFB			7591+	VCH	V21, V22, V23, 3, 1	test instruction
00009D76	B98D 0020			7592+	EPSW	R2, R0	extract psw
00009D7A	5020 500C		0000000C	7593+	ST	R2, CCPSW	to save CC
00009D7E	E750 5048 080E		00009D38	7594+	VST	V21, V10180	save v1 output
00009D84	07FB			7595+	BR	R11	return
00009D88				7596+RE180	DC	0F	V1 for this test
00009D88				7597+	DROP	R5	
00009D88	00000000	00000000		7598	DC	XL16' 0000000000000000 0000000000000000'	result
00009D90	00000000	00000000					
00009D98	00010003	04050607		7599	DC	XL16' 0001000304050607 00090A0B0C0D0E0F'	v2
00009DA0	00090A0B	0C0D0E0F					
00009DA8	01110233	11550677		7600	DC	XL16' 0111023311550677 1179116B514D312F'	v3
00009DB0	1179116B	514D312F					
				7601			
00009DB8				7602	VRR_B	VCHL, 3, 3	
00009DB8		00009DB8		7603+	DS	0FD	
00009DB8	00009E20			7604+	USING	*, R5	base for test data and test routine
00009DBC	00B5			7605+T181	DC	A(X181)	address of test routine
00009DBE	00			7606+	DC	H' 181'	test number
00009DBE	00			7607+	DC	X' 00'	
00009DBF	03			7608+	DC	HL1' 3'	m4 used
00009DC0	01			7609+	DC	HL1' 1'	m5 used
00009DC1	03			7610+	DC	HL1' 3'	CC
00009DC2	0E			7611+	DC	HL1' 14'	CC failed mask
00009DC4	00000000	00000000		7612+	DS	2F	extracted PSW after test (has CC)
00009DCC	FF			7613+	DC	X' FF'	extracted CC, if test failed
00009DCD	E5C3C8D3	40404040		7614+	DC	CL8' VCHL'	instruction name
00009DD8	00009E50			7615+	DC	A(RE181)	address of v1 result
00009DDC	00009E60			7616+	DC	A(RE181+16)	address of v2 source
00009DE0	00009E70			7617+	DC	A(RE181+32)	address of v3 source
00009DE4	00000010			7618+	DC	A(16)	result length
00009DE8	00009E50			7619+REA181	DC	A(RE181)	result address
00009DF0	00000000	00000000		7620+	DS	2FD	gap
00009DF8	00000000	00000000					

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00009E00	00000000 00000000			7621+V10181	DS	XL16	V1 output
00009E08	00000000 00000000						
00009E10	00000000 00000000			7622+	DS	2FD	gap
00009E18	00000000 00000000						
				7623+*			
00009E20				7624+X181	DS	0F	
00009E20	E310 5024 0014		00000024	7625+	LGF	R1, V2ADDR	load v2 source
00009E26	E761 0000 0806		00000000	7626+	VL	v22, 0(R1)	use v21 to test decoder
00009E2C	E310 5028 0014		00000028	7627+	LGF	R1, V3ADDR	load v3 source
00009E32	E771 0000 0806		00000000	7628+	VL	v23, 0(R1)	use v22 to test decoder
00009E38	E756 7010 3EF9			7629+	VCHL	V21, V22, V23, 3, 1	test instruction
00009E3E	B98D 0020			7630+	EPSW	R2, R0	extract psw
00009E42	5020 500C		0000000C	7631+	ST	R2, CCPSW	to save CC
00009E46	E750 5048 080E		00009E00	7632+	VST	V21, V10181	save v1 output
00009E4C	07FB			7633+	BR	R11	return
00009E50				7634+RE181	DC	0F	V1 for this test
00009E50				7635+	DROP	R5	
00009E50	00000000 00000000			7636	DC	XL16' 0000000000000000 0000000000000000'	result
00009E58	00000000 00000000						
00009E60	08090A0B 0C0D0E0F			7637	DC	XL16' 08090A0B0C0D0E0F 0001020304050607'	v2
00009E68	00010203 04050607						
00009E70	1179116B 514D312F			7638	DC	XL16' 1179116B514D312F 0111023311550677'	v3
00009E78	01110233 11550677						
				7639			
				7640	VRR_B	VCH, 3, 3	
00009E80				7641+	DS	0FD	
00009E80		00009E80		7642+	USING	*, R5	base for test data and test routine
00009E80	00009EE8			7643+T182	DC	A(X182)	address of test routine
00009E84	00B6			7644+	DC	H' 182'	test number
00009E86	00			7645+	DC	X' 00'	
00009E87	03			7646+	DC	HL1' 3'	m4 used
00009E88	01			7647+	DC	HL1' 1'	m5 used
00009E89	03			7648+	DC	HL1' 3'	CC
00009E8A	0E			7649+	DC	HL1' 14'	CC failed mask
00009E8C	00000000 00000000			7650+	DS	2F	extracted PSW after test (has CC)
00009E94	FF			7651+	DC	X' FF'	extracted CC, if test failed
00009E95	E5C3C840 40404040			7652+	DC	CL8' VCH'	instruction name
00009EA0	00009F18			7653+	DC	A(RE182)	address of v1 result
00009EA4	00009F28			7654+	DC	A(RE182+16)	address of v2 source
00009EA8	00009F38			7655+	DC	A(RE182+32)	address of v3 source
00009EAC	00000010			7656+	DC	A(16)	result length
00009EB0	00009F18			7657+REA182	DC	A(RE182)	result address
00009EB8	00000000 00000000			7658+	DS	2FD	gap
00009EC0	00000000 00000000						
00009EC8	00000000 00000000			7659+V10182	DS	XL16	V1 output
00009ED0	00000000 00000000						
00009ED8	00000000 00000000			7660+	DS	2FD	gap
00009EE0	00000000 00000000						
				7661+*			
00009EE8				7662+X182	DS	0F	
00009EE8	E310 5024 0014		00000024	7663+	LGF	R1, V2ADDR	load v2 source
00009EEE	E761 0000 0806		00000000	7664+	VL	v22, 0(R1)	use v21 to test decoder
00009EF4	E310 5028 0014		00000028	7665+	LGF	R1, V3ADDR	load v3 source
00009EFA	E771 0000 0806		00000000	7666+	VL	v23, 0(R1)	use v22 to test decoder
00009F00	E756 7010 3EFB			7667+	VCH	V21, V22, V23, 3, 1	test instruction
00009F06	B98D 0020			7668+	EPSW	R2, R0	extract psw

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				7682 *	
				7683 * table of pointers to individual tests	
				7684 *	
00009F50				7685 E7TESTS DS OF	
				7686 PTTABLE	
00009F50				7687+TTABLE DS OF	
00009F50	00001118			7688+	DC A(T1) test address
00009F54	000011E0			7689+	DC A(T2) test address
00009F58	000012A8			7690+	DC A(T3) test address
00009F5C	00001370			7691+	DC A(T4) test address
00009F60	00001438			7692+	DC A(T5) test address
00009F64	00001500			7693+	DC A(T6) test address
00009F68	000015C8			7694+	DC A(T7) test address
00009F6C	00001690			7695+	DC A(T8) test address
00009F70	00001758			7696+	DC A(T9) test address
00009F74	00001820			7697+	DC A(T10) test address
00009F78	000018E8			7698+	DC A(T11) test address
00009F7C	000019B0			7699+	DC A(T12) test address
00009F80	00001A78			7700+	DC A(T13) test address
00009F84	00001B40			7701+	DC A(T14) test address
00009F88	00001C08			7702+	DC A(T15) test address
00009F8C	00001CD0			7703+	DC A(T16) test address
00009F90	00001D98			7704+	DC A(T17) test address
00009F94	00001E60			7705+	DC A(T18) test address
00009F98	00001F28			7706+	DC A(T19) test address
00009F9C	00001FF0			7707+	DC A(T20) test address
00009FA0	000020B8			7708+	DC A(T21) test address
00009FA4	00002180			7709+	DC A(T22) test address
00009FA8	00002248			7710+	DC A(T23) test address
00009FAC	00002310			7711+	DC A(T24) test address
00009FB0	000023D8			7712+	DC A(T25) test address
00009FB4	000024A0			7713+	DC A(T26) test address
00009FB8	00002568			7714+	DC A(T27) test address
00009FBC	00002630			7715+	DC A(T28) test address
00009FC0	000026F8			7716+	DC A(T29) test address
00009FC4	000027C0			7717+	DC A(T30) test address
00009FC8	00002888			7718+	DC A(T31) test address
00009FCC	00002950			7719+	DC A(T32) test address
00009FD0	00002A18			7720+	DC A(T33) test address
00009FD4	00002AE0			7721+	DC A(T34) test address
00009FD8	00002BA8			7722+	DC A(T35) test address
00009FDC	00002C70			7723+	DC A(T36) test address
00009FE0	00002D38			7724+	DC A(T37) test address
00009FE4	00002E00			7725+	DC A(T38) test address
00009FE8	00002EC8			7726+	DC A(T39) test address
00009FEC	00002F90			7727+	DC A(T40) test address
00009FF0	00003058			7728+	DC A(T41) test address
00009FF4	00003120			7729+	DC A(T42) test address
00009FF8	000031E8			7730+	DC A(T43) test address
00009FFC	000032B0			7731+	DC A(T44) test address
0000A000	00003378			7732+	DC A(T45) test address
0000A004	00003440			7733+	DC A(T46) test address
0000A008	00003508			7734+	DC A(T47) test address
0000A00C	000035D0			7735+	DC A(T48) test address
0000A010	00003698			7736+	DC A(T49) test address
0000A014	00003760			7737+	DC A(T50) test address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000A018	00003828			7738+	DC	A(T51)	test address
0000A01C	000038F0			7739+	DC	A(T52)	test address
0000A020	000039B8			7740+	DC	A(T53)	test address
0000A024	00003A80			7741+	DC	A(T54)	test address
0000A028	00003B48			7742+	DC	A(T55)	test address
0000A02C	00003C10			7743+	DC	A(T56)	test address
0000A030	00003CD8			7744+	DC	A(T57)	test address
0000A034	00003DA0			7745+	DC	A(T58)	test address
0000A038	00003E68			7746+	DC	A(T59)	test address
0000A03C	00003F30			7747+	DC	A(T60)	test address
0000A040	00003FF8			7748+	DC	A(T61)	test address
0000A044	000040C0			7749+	DC	A(T62)	test address
0000A048	00004188			7750+	DC	A(T63)	test address
0000A04C	00004250			7751+	DC	A(T64)	test address
0000A050	00004318			7752+	DC	A(T65)	test address
0000A054	000043E0			7753+	DC	A(T66)	test address
0000A058	000044A8			7754+	DC	A(T67)	test address
0000A05C	00004570			7755+	DC	A(T68)	test address
0000A060	00004638			7756+	DC	A(T69)	test address
0000A064	00004700			7757+	DC	A(T70)	test address
0000A068	000047C8			7758+	DC	A(T71)	test address
0000A06C	00004890			7759+	DC	A(T72)	test address
0000A070	00004958			7760+	DC	A(T73)	test address
0000A074	00004A20			7761+	DC	A(T74)	test address
0000A078	00004AE8			7762+	DC	A(T75)	test address
0000A07C	00004BB0			7763+	DC	A(T76)	test address
0000A080	00004C78			7764+	DC	A(T77)	test address
0000A084	00004D40			7765+	DC	A(T78)	test address
0000A088	00004E08			7766+	DC	A(T79)	test address
0000A08C	00004ED0			7767+	DC	A(T80)	test address
0000A090	00004F98			7768+	DC	A(T81)	test address
0000A094	00005060			7769+	DC	A(T82)	test address
0000A098	00005128			7770+	DC	A(T83)	test address
0000A09C	000051F0			7771+	DC	A(T84)	test address
0000A0A0	000052B8			7772+	DC	A(T85)	test address
0000A0A4	00005380			7773+	DC	A(T86)	test address
0000A0A8	00005448			7774+	DC	A(T87)	test address
0000A0AC	00005510			7775+	DC	A(T88)	test address
0000A0B0	000055D8			7776+	DC	A(T89)	test address
0000A0B4	000056A0			7777+	DC	A(T90)	test address
0000A0B8	00005768			7778+	DC	A(T91)	test address
0000A0BC	00005830			7779+	DC	A(T92)	test address
0000A0C0	000058F8			7780+	DC	A(T93)	test address
0000A0C4	000059C0			7781+	DC	A(T94)	test address
0000A0C8	00005A88			7782+	DC	A(T95)	test address
0000A0CC	00005B50			7783+	DC	A(T96)	test address
0000A0D0	00005C18			7784+	DC	A(T97)	test address
0000A0D4	00005CE0			7785+	DC	A(T98)	test address
0000A0D8	00005DA8			7786+	DC	A(T99)	test address
0000A0DC	00005E70			7787+	DC	A(T100)	test address
0000A0E0	00005F38			7788+	DC	A(T101)	test address
0000A0E4	00006000			7789+	DC	A(T102)	test address
0000A0E8	000060C8			7790+	DC	A(T103)	test address
0000A0EC	00006190			7791+	DC	A(T104)	test address
0000A0F0	00006258			7792+	DC	A(T105)	test address
0000A0F4	00006320			7793+	DC	A(T106)	test address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
0000A0F8	000063E8			7794+	DC	A(T107) test address
0000A0FC	000064B0			7795+	DC	A(T108) test address
0000A100	00006578			7796+	DC	A(T109) test address
0000A104	00006640			7797+	DC	A(T110) test address
0000A108	00006708			7798+	DC	A(T111) test address
0000A10C	000067D0			7799+	DC	A(T112) test address
0000A110	00006898			7800+	DC	A(T113) test address
0000A114	00006960			7801+	DC	A(T114) test address
0000A118	00006A28			7802+	DC	A(T115) test address
0000A11C	00006AF0			7803+	DC	A(T116) test address
0000A120	00006BB8			7804+	DC	A(T117) test address
0000A124	00006C80			7805+	DC	A(T118) test address
0000A128	00006D48			7806+	DC	A(T119) test address
0000A12C	00006E10			7807+	DC	A(T120) test address
0000A130	00006ED8			7808+	DC	A(T121) test address
0000A134	00006FA0			7809+	DC	A(T122) test address
0000A138	00007068			7810+	DC	A(T123) test address
0000A13C	00007130			7811+	DC	A(T124) test address
0000A140	000071F8			7812+	DC	A(T125) test address
0000A144	000072C0			7813+	DC	A(T126) test address
0000A148	00007388			7814+	DC	A(T127) test address
0000A14C	00007450			7815+	DC	A(T128) test address
0000A150	00007518			7816+	DC	A(T129) test address
0000A154	000075E0			7817+	DC	A(T130) test address
0000A158	000076A8			7818+	DC	A(T131) test address
0000A15C	00007770			7819+	DC	A(T132) test address
0000A160	00007838			7820+	DC	A(T133) test address
0000A164	00007900			7821+	DC	A(T134) test address
0000A168	000079C8			7822+	DC	A(T135) test address
0000A16C	00007A90			7823+	DC	A(T136) test address
0000A170	00007B58			7824+	DC	A(T137) test address
0000A174	00007C20			7825+	DC	A(T138) test address
0000A178	00007CE8			7826+	DC	A(T139) test address
0000A17C	00007DB0			7827+	DC	A(T140) test address
0000A180	00007E78			7828+	DC	A(T141) test address
0000A184	00007F40			7829+	DC	A(T142) test address
0000A188	00008008			7830+	DC	A(T143) test address
0000A18C	000080D0			7831+	DC	A(T144) test address
0000A190	00008198			7832+	DC	A(T145) test address
0000A194	00008260			7833+	DC	A(T146) test address
0000A198	00008328			7834+	DC	A(T147) test address
0000A19C	000083F0			7835+	DC	A(T148) test address
0000A1A0	000084B8			7836+	DC	A(T149) test address
0000A1A4	00008580			7837+	DC	A(T150) test address
0000A1A8	00008648			7838+	DC	A(T151) test address
0000A1AC	00008710			7839+	DC	A(T152) test address
0000A1B0	000087D8			7840+	DC	A(T153) test address
0000A1B4	000088A0			7841+	DC	A(T154) test address
0000A1B8	00008968			7842+	DC	A(T155) test address
0000A1BC	00008A30			7843+	DC	A(T156) test address
0000A1C0	00008AF8			7844+	DC	A(T157) test address
0000A1C4	00008BC0			7845+	DC	A(T158) test address
0000A1C8	00008C88			7846+	DC	A(T159) test address
0000A1CC	00008D50			7847+	DC	A(T160) test address
0000A1D0	00008E18			7848+	DC	A(T161) test address
0000A1D4	00008EE0			7849+	DC	A(T162) test address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000A1D8	00008FA8			7850+	DC	A(T163)	test address
0000A1DC	00009070			7851+	DC	A(T164)	test address
0000A1E0	00009138			7852+	DC	A(T165)	test address
0000A1E4	00009200			7853+	DC	A(T166)	test address
0000A1E8	000092C8			7854+	DC	A(T167)	test address
0000A1EC	00009390			7855+	DC	A(T168)	test address
0000A1F0	00009458			7856+	DC	A(T169)	test address
0000A1F4	00009520			7857+	DC	A(T170)	test address
0000A1F8	000095E8			7858+	DC	A(T171)	test address
0000A1FC	000096B0			7859+	DC	A(T172)	test address
0000A200	00009778			7860+	DC	A(T173)	test address
0000A204	00009840			7861+	DC	A(T174)	test address
0000A208	00009908			7862+	DC	A(T175)	test address
0000A20C	000099D0			7863+	DC	A(T176)	test address
0000A210	00009A98			7864+	DC	A(T177)	test address
0000A214	00009B60			7865+	DC	A(T178)	test address
0000A218	00009C28			7866+	DC	A(T179)	test address
0000A21C	00009CF0			7867+	DC	A(T180)	test address
0000A220	00009DB8			7868+	DC	A(T181)	test address
0000A224	00009E80			7869+	DC	A(T182)	test address
				7870+*			
0000A228	00000000			7871+	DC	A(0)	end of table
0000A22C	00000000			7872+	DC	A(0)	end of table
				7873			
0000A230	00000000			7874	DC	F' 0'	END OF TABLE
0000A234	00000000			7875	DC	F' 0'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				7877	*****
				7878	* Register equates
				7879	*****
		00000000	00000001	7881 R0	EQU 0
		00000001	00000001	7882 R1	EQU 1
		00000002	00000001	7883 R2	EQU 2
		00000003	00000001	7884 R3	EQU 3
		00000004	00000001	7885 R4	EQU 4
		00000005	00000001	7886 R5	EQU 5
		00000006	00000001	7887 R6	EQU 6
		00000007	00000001	7888 R7	EQU 7
		00000008	00000001	7889 R8	EQU 8
		00000009	00000001	7890 R9	EQU 9
		0000000A	00000001	7891 R10	EQU 10
		0000000B	00000001	7892 R11	EQU 11
		0000000C	00000001	7893 R12	EQU 12
		0000000D	00000001	7894 R13	EQU 13
		0000000E	00000001	7895 R14	EQU 14
		0000000F	00000001	7896 R15	EQU 15
				7898	*****
				7899	* Register equates
				7900	*****
		00000000	00000001	7902 V0	EQU 0
		00000001	00000001	7903 V1	EQU 1
		00000002	00000001	7904 V2	EQU 2
		00000003	00000001	7905 V3	EQU 3
		00000004	00000001	7906 V4	EQU 4
		00000005	00000001	7907 V5	EQU 5
		00000006	00000001	7908 V6	EQU 6
		00000007	00000001	7909 V7	EQU 7
		00000008	00000001	7910 V8	EQU 8
		00000009	00000001	7911 V9	EQU 9
		0000000A	00000001	7912 V10	EQU 10
		0000000B	00000001	7913 V11	EQU 11
		0000000C	00000001	7914 V12	EQU 12
		0000000D	00000001	7915 V13	EQU 13
		0000000E	00000001	7916 V14	EQU 14
		0000000F	00000001	7917 V15	EQU 15
		00000010	00000001	7918 V16	EQU 16
		00000011	00000001	7919 V17	EQU 17
		00000012	00000001	7920 V18	EQU 18
		00000013	00000001	7921 V19	EQU 19
		00000014	00000001	7922 V20	EQU 20
		00000015	00000001	7923 V21	EQU 21

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
PRT3	C	000010C0	18	500	265	266	267	274	275	276	281	282	283	303	304	305	312
					313	314	319	320	321								
PRTLNE	C	00001008	16	464	474	324											
PRTLNG	U	0000004D	1	474	323												
PRTM4	C	00001044	3	469	314												
PRTM5	C	00001051	3	472	321												
PRTNAME	C	00001033	8	467	307												
PRTNUM	C	00001018	3	465	305												
R0	U	00000000	1	7881	121	171	174	194	196	197	198	203	222	223	285	289	290
					323	331	332	357	359	375	378	380	382	384	399	699	737
					775	814	852	890	929	967	1005	1047	1085	1123	1161	1199	1237
					1276	1314	1352	1390	1428	1466	1505	1543	1581	1619	1657	1695	1735
					1773	1811	1859	1897	1935	1974	2012	2050	2089	2127	2165	2207	2245
					2283	2321	2359	2397	2435	2473	2512	2550	2588	2626	2664	2702	2740
					2778	2817	2855	2893	2931	2969	3007	3045	3083	3124	3162	3200	3248
					3286	3324	3363	3401	3439	3478	3516	3554	3593	3631	3669	3711	3749
					3787	3825	3863	3901	3940	3978	4016	4054	4092	4130	4169	4207	4245
					4283	4321	4359	4398	4436	4474	4512	4550	4588	4636	4674	4712	4751
					4789	4827	4866	4904	4942	4981	5019	5057	5099	5137	5175	5213	5251
					5289	5328	5366	5404	5442	5480	5518	5557	5595	5633	5671	5709	5747
					5786	5824	5862	5900	5938	5976	6024	6062	6100	6139	6177	6215	6254
					6292	6330	6369	6407	6445	6487	6525	6563	6601	6639	6677	6715	6753
					6792	6830	6868	6906	6944	6982	7020	7058	7097	7135	7173	7211	7249
					7287	7325	7363	7402	7440	7478	7516	7554	7592	7630	7668		
R1	U	00000001	1	7882	204	229	230	231	234	235	250	251	256	257	258	259	286
					324	341	342	389	403	694	695	696	697	732	733	734	735
					770	771	772	773	809	810	811	812	847	848	849	850	885
					886	887	888	924	925	926	927	962	963	964	965	1000	1001
					1002	1003	1042	1043	1044	1045	1080	1081	1082	1083	1118	1119	1120
					1121	1156	1157	1158	1159	1194	1195	1196	1197	1232	1233	1234	1235
					1271	1272	1273	1274	1309	1310	1311	1312	1347	1348	1349	1350	1385
					1386	1387	1388	1423	1424	1425	1426	1461	1462	1463	1464	1500	1501
					1502	1503	1538	1539	1540	1541	1576	1577	1578	1579	1614	1615	1616
					1617	1652	1653	1654	1655	1690	1691	1692	1693	1730	1731	1732	1733
					1768	1769	1770	1771	1806	1807	1808	1809	1854	1855	1856	1857	1892
					1893	1894	1895	1930	1931	1932	1933	1969	1970	1971	1972	2007	2008
					2009	2010	2045	2046	2047	2048	2084	2085	2086	2087	2122	2123	2124
					2125	2160	2161	2162	2163	2202	2203	2204	2205	2240	2241	2242	2243
					2278	2279	2280	2281	2316	2317	2318	2319	2354	2355	2356	2357	2392
					2393	2394	2395	2430	2431	2432	2433	2468	2469	2470	2471	2507	2508
					2509	2510	2545	2546	2547	2548	2583	2584	2585	2586	2621	2622	2623
					2624	2659	2660	2661	2662	2697	2698	2699	2700	2735	2736	2737	2738
					2773	2774	2775	2776	2812	2813	2814	2815	2850	2851	2852	2853	2888
					2889	2890	2891	2926	2927	2928	2929	2964	2965	2966	2967	3002	3003
					3004	3005	3040	3041	3042	3043	3078	3079	3080	3081	3119	3120	3121
					3122	3157	3158	3159	3160	3195	3196	3197	3198	3243	3244	3245	3246
					3281	3282	3283	3284	3319	3320	3321	3322	3358	3359	3360	3361	3396
					3397	3398	3399	3434	3435	3436	3437	3473	3474	3475	3476	3511	3512
					3513	3514	3549	3550	3551	3552	3588	3589	3590	3591	3626	3627	3628
					3629	3664	3665	3666	3667	3706	3707	3708	3709	3744	3745	3746	3747
					3782	3783	3784	3785	3820	3821	3822	3823	3858	3859	3860	3861	3896
					3897	3898	3899	3935	3936	3937	3938	3973	3974	3975	3976	4011	4012
					4013	4014	4049	4050	4051	4052	4087	4088	4089	4090	4125	4126	4127
					4128	4164	4165	4166	4167	4202	4203	4204	4205	4240	4241	4242	4243
					4278	4279	4280	4281	4316	4317	4318	4319	4354	4355	4356	4357	4393
					4394	4395	4396	4431	4432	4433	4434	4469	4470	4471	4472	4507	4508

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					4509	4510	4545	4546	4547	4548	4583	4584	4585	4586	4631	4632	4633
					4634	4669	4670	4671	4672	4707	4708	4709	4710	4746	4747	4748	4749
					4784	4785	4786	4787	4822	4823	4824	4825	4861	4862	4863	4864	4899
					4900	4901	4902	4937	4938	4939	4940	4976	4977	4978	4979	5014	5015
					5016	5017	5052	5053	5054	5055	5094	5095	5096	5097	5132	5133	5134
					5135	5170	5171	5172	5173	5208	5209	5210	5211	5246	5247	5248	5249
					5284	5285	5286	5287	5323	5324	5325	5326	5361	5362	5363	5364	5399
					5400	5401	5402	5437	5438	5439	5440	5475	5476	5477	5478	5513	5514
					5515	5516	5552	5553	5554	5555	5590	5591	5592	5593	5628	5629	5630
					5631	5666	5667	5668	5669	5704	5705	5706	5707	5742	5743	5744	5745
					5781	5782	5783	5784	5819	5820	5821	5822	5857	5858	5859	5860	5895
					5896	5897	5898	5933	5934	5935	5936	5971	5972	5973	5974	6019	6020
					6021	6022	6057	6058	6059	6060	6095	6096	6097	6098	6134	6135	6136
					6137	6172	6173	6174	6175	6210	6211	6212	6213	6249	6250	6251	6252
					6287	6288	6289	6290	6325	6326	6327	6328	6364	6365	6366	6367	6402
					6403	6404	6405	6440	6441	6442	6443	6482	6483	6484	6485	6520	6521
					6522	6523	6558	6559	6560	6561	6596	6597	6598	6599	6634	6635	6636
					6637	6672	6673	6674	6675	6710	6711	6712	6713	6748	6749	6750	6751
					6787	6788	6789	6790	6825	6826	6827	6828	6863	6864	6865	6866	6901
					6902	6903	6904	6939	6940	6941	6942	6977	6978	6979	6980	7015	7016
					7017	7018	7053	7054	7055	7056	7092	7093	7094	7095	7130	7131	7132
					7133	7168	7169	7170	7171	7206	7207	7208	7209	7244	7245	7246	7247
					7282	7283	7284	7285	7320	7321	7322	7323	7358	7359	7360	7361	7397
					7398	7399	7400	7435	7436	7437	7438	7473	7474	7475	7476	7511	7512
					7513	7514	7549	7550	7551	7552	7587	7588	7589	7590	7625	7626	7627
					7628	7663	7664	7665	7666								
R10	U	0000000A	1	7891	159	168	169										
R11	U	0000000B	1	7892	226	227	702	740	778	817	855	893	932	970	1008	1050	1088
					1126	1164	1202	1240	1279	1317	1355	1393	1431	1469	1508	1546	1584
					1622	1660	1698	1738	1776	1814	1862	1900	1938	1977	2015	2053	2092
					2130	2168	2210	2248	2286	2324	2362	2400	2438	2476	2515	2553	2591
					2629	2667	2705	2743	2781	2820	2858	2896	2934	2972	3010	3048	3086
					3127	3165	3203	3251	3289	3327	3366	3404	3442	3481	3519	3557	3596
					3634	3672	3714	3752	3790	3828	3866	3904	3943	3981	4019	4057	4095
					4133	4172	4210	4248	4286	4324	4362	4401	4439	4477	4515	4553	4591
					4639	4677	4715	4754	4792	4830	4869	4907	4945	4984	5022	5060	5102
					5140	5178	5216	5254	5292	5331	5369	5407	5445	5483	5521	5560	5598
					5636	5674	5712	5750	5789	5827	5865	5903	5941	5979	6027	6065	6103
					6142	6180	6218	6257	6295	6333	6372	6410	6448	6490	6528	6566	6604
					6642	6680	6718	6756	6795	6833	6871	6909	6947	6985	7023	7061	7100
					7138	7176	7214	7252	7290	7328	7366	7405	7443	7481	7519	7557	7595
					7633	7671											
R12	U	0000000C	1	7893	213	216	238	334									
R13	U	0000000D	1	7894													
R14	U	0000000E	1	7895													
R15	U	0000000F	1	7896	287	325	352	362	363								
R2	U	00000002	1	7883	205	263	264	271	272	273	278	279	280	301	302	309	310
					311	316	317	318	357	358	359	376	378	384	385	386	388
					394	399	400	699	700	737	738	775	776	814	815	852	853
					890	891	929	930	967	968	1005	1006	1047	1048	1085	1086	1123
					1124	1161	1162	1199	1200	1237	1238	1276	1277	1314	1315	1352	1353
					1390	1391	1428	1429	1466	1467	1505	1506	1543	1544	1581	1582	1619
					1620	1657	1658	1695	1696	1735	1736	1773	1774	1811	1812	1859	1860
					1897	1898	1935	1936	1974	1975	2012	2013	2050	2051	2089	2090	2127
					2128	2165	2166	2207	2208	2245	2246	2283	2284	2321	2322	2359	2360
					2397	2398	2435	2436	2473	2474	2512	2513	2550	2551	2588	2589	2626

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					2627	2664	2665	2702	2703	2740	2741	2778	2779	2817	2818	2855	2856
					2893	2894	2931	2932	2969	2970	3007	3008	3045	3046	3083	3084	3124
					3125	3162	3163	3200	3201	3248	3249	3286	3287	3324	3325	3363	3364
					3401	3402	3439	3440	3478	3479	3516	3517	3554	3555	3593	3594	3631
					3632	3669	3670	3711	3712	3749	3750	3787	3788	3825	3826	3863	3864
					3901	3902	3940	3941	3978	3979	4016	4017	4054	4055	4092	4093	4130
					4131	4169	4170	4207	4208	4245	4246	4283	4284	4321	4322	4359	4360
					4398	4399	4436	4437	4474	4475	4512	4513	4550	4551	4588	4589	4636
					4637	4674	4675	4712	4713	4751	4752	4789	4790	4827	4828	4866	4867
					4904	4905	4942	4943	4981	4982	5019	5020	5057	5058	5099	5100	5137
					5138	5175	5176	5213	5214	5251	5252	5289	5290	5328	5329	5366	5367
					5404	5405	5442	5443	5480	5481	5518	5519	5557	5558	5595	5596	5633
					5634	5671	5672	5709	5710	5747	5748	5786	5787	5824	5825	5862	5863
					5900	5901	5938	5939	5976	5977	6024	6025	6062	6063	6100	6101	6139
					6140	6177	6178	6215	6216	6254	6255	6292	6293	6330	6331	6369	6370
					6407	6408	6445	6446	6487	6488	6525	6526	6563	6564	6601	6602	6639
					6640	6677	6678	6715	6716	6753	6754	6792	6793	6830	6831	6868	6869
					6906	6907	6944	6945	6982	6983	7020	7021	7058	7059	7097	7098	7135
					7136	7173	7174	7211	7212	7249	7250	7287	7288	7325	7326	7363	7364
					7402	7403	7440	7441	7478	7479	7516	7517	7554	7555	7592	7593	7630
					7631	7668	7669										
R3	U	00000003	1	7884													
R4	U	00000004	1	7885													
R5	U	00000005	1	7886	216	217	220	353	361	673	704	711	742	749	780	788	819
					826	857	864	895	903	934	941	972	979	1010	1021	1052	1059
					1090	1097	1128	1135	1166	1173	1204	1211	1242	1250	1281	1288	1319
					1326	1357	1364	1395	1402	1433	1440	1471	1479	1510	1517	1548	1555
					1586	1593	1624	1631	1662	1669	1700	1709	1740	1747	1778	1785	1816
					1833	1864	1871	1902	1909	1940	1948	1979	1986	2017	2024	2055	2063
					2094	2101	2132	2139	2170	2181	2212	2219	2250	2257	2288	2295	2326
					2333	2364	2371	2402	2409	2440	2447	2478	2486	2517	2524	2555	2562
					2593	2600	2631	2638	2669	2676	2707	2714	2745	2752	2783	2791	2822
					2829	2860	2867	2898	2905	2936	2943	2974	2981	3012	3019	3050	3057
					3088	3098	3129	3136	3167	3174	3205	3222	3253	3260	3291	3298	3329
					3337	3368	3375	3406	3413	3444	3452	3483	3490	3521	3528	3559	3567
					3598	3605	3636	3643	3674	3685	3716	3723	3754	3761	3792	3799	3830
					3837	3868	3875	3906	3914	3945	3952	3983	3990	4021	4028	4059	4066
					4097	4104	4135	4143	4174	4181	4212	4219	4250	4257	4288	4295	4326
					4333	4364	4372	4403	4410	4441	4448	4479	4486	4517	4524	4555	4562
					4593	4610	4641	4648	4679	4686	4717	4725	4756	4763	4794	4801	4832
					4840	4871	4878	4909	4916	4947	4955	4986	4993	5024	5031	5062	5073
					5104	5111	5142	5149	5180	5187	5218	5225	5256	5263	5294	5302	5333
					5340	5371	5378	5409	5416	5447	5454	5485	5492	5523	5531	5562	5569
					5600	5607	5638	5645	5676	5683	5714	5721	5752	5760	5791	5798	5829
					5836	5867	5874	5905	5912	5943	5950	5981	5998	6029	6036	6067	6074
					6105	6113	6144	6151	6182	6189	6220	6228	6259	6266	6297	6304	6335
					6343	6374	6381	6412	6419	6450	6461	6492	6499	6530	6537	6568	6575
					6606	6613	6644	6651	6682	6689	6720	6727	6758	6766	6797	6804	6835
					6842	6873	6880	6911	6918	6949	6956	6987	6994	7025	7032	7063	7071
					7102	7109	7140	7147	7178	7185	7216	7223	7254	7261	7292	7299	7330
					7337	7368	7376	7407	7414	7445	7452	7483	7490	7521	7528	7559	7566
					7597	7604	7635	7642	7673								
R6	U	00000006	1	7887													
R7	U	00000007	1	7888													
R8	U	00000008	1	7889	157	161	162	163	165								
R9	U	00000009	1	7890	158	165	166	168									

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE1	F	000011B0	4	703	684 685 686 688
RE10	F	000018B8	4	1051	1032 1033 1034 1036
RE100	F	00005F08	4	4516	4497 4498 4499 4501
RE101	F	00005FD0	4	4554	4535 4536 4537 4539
RE102	F	00006098	4	4592	4573 4574 4575 4577
RE103	F	00006160	4	4640	4621 4622 4623 4625
RE104	F	00006228	4	4678	4659 4660 4661 4663
RE105	F	000062F0	4	4716	4697 4698 4699 4701
RE106	F	000063B8	4	4755	4736 4737 4738 4740
RE107	F	00006480	4	4793	4774 4775 4776 4778
RE108	F	00006548	4	4831	4812 4813 4814 4816
RE109	F	00006610	4	4870	4851 4852 4853 4855
RE11	F	00001980	4	1089	1070 1071 1072 1074
RE110	F	000066D8	4	4908	4889 4890 4891 4893
RE111	F	000067A0	4	4946	4927 4928 4929 4931
RE112	F	00006868	4	4985	4966 4967 4968 4970
RE113	F	00006930	4	5023	5004 5005 5006 5008
RE114	F	000069F8	4	5061	5042 5043 5044 5046
RE115	F	00006AC0	4	5103	5084 5085 5086 5088
RE116	F	00006B88	4	5141	5122 5123 5124 5126
RE117	F	00006C50	4	5179	5160 5161 5162 5164
RE118	F	00006D18	4	5217	5198 5199 5200 5202
RE119	F	00006DE0	4	5255	5236 5237 5238 5240
RE12	F	00001A48	4	1127	1108 1109 1110 1112
RE120	F	00006EA8	4	5293	5274 5275 5276 5278
RE121	F	00006F70	4	5332	5313 5314 5315 5317
RE122	F	00007038	4	5370	5351 5352 5353 5355
RE123	F	00007100	4	5408	5389 5390 5391 5393
RE124	F	000071C8	4	5446	5427 5428 5429 5431
RE125	F	00007290	4	5484	5465 5466 5467 5469
RE126	F	00007358	4	5522	5503 5504 5505 5507
RE127	F	00007420	4	5561	5542 5543 5544 5546
RE128	F	000074E8	4	5599	5580 5581 5582 5584
RE129	F	000075B0	4	5637	5618 5619 5620 5622
RE13	F	00001B10	4	1165	1146 1147 1148 1150
RE130	F	00007678	4	5675	5656 5657 5658 5660
RE131	F	00007740	4	5713	5694 5695 5696 5698
RE132	F	00007808	4	5751	5732 5733 5734 5736
RE133	F	000078D0	4	5790	5771 5772 5773 5775
RE134	F	00007998	4	5828	5809 5810 5811 5813
RE135	F	00007A60	4	5866	5847 5848 5849 5851
RE136	F	00007B28	4	5904	5885 5886 5887 5889
RE137	F	00007BF0	4	5942	5923 5924 5925 5927
RE138	F	00007CB8	4	5980	5961 5962 5963 5965
RE139	F	00007D80	4	6028	6009 6010 6011 6013
RE14	F	00001BD8	4	1203	1184 1185 1186 1188
RE140	F	00007E48	4	6066	6047 6048 6049 6051
RE141	F	00007F10	4	6104	6085 6086 6087 6089
RE142	F	00007FD8	4	6143	6124 6125 6126 6128
RE143	F	000080A0	4	6181	6162 6163 6164 6166
RE144	F	00008168	4	6219	6200 6201 6202 6204
RE145	F	00008230	4	6258	6239 6240 6241 6243
RE146	F	000082F8	4	6296	6277 6278 6279 6281
RE147	F	000083C0	4	6334	6315 6316 6317 6319
RE148	F	00008488	4	6373	6354 6355 6356 6358
RE149	F	00008550	4	6411	6392 6393 6394 6396

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE15	F	00001CA0	4	1241	1222 1223 1224 1226
RE150	F	00008618	4	6449	6430 6431 6432 6434
RE151	F	000086E0	4	6491	6472 6473 6474 6476
RE152	F	000087A8	4	6529	6510 6511 6512 6514
RE153	F	00008870	4	6567	6548 6549 6550 6552
RE154	F	00008938	4	6605	6586 6587 6588 6590
RE155	F	00008A00	4	6643	6624 6625 6626 6628
RE156	F	00008AC8	4	6681	6662 6663 6664 6666
RE157	F	00008B90	4	6719	6700 6701 6702 6704
RE158	F	00008C58	4	6757	6738 6739 6740 6742
RE159	F	00008D20	4	6796	6777 6778 6779 6781
RE16	F	00001D68	4	1280	1261 1262 1263 1265
RE160	F	00008DE8	4	6834	6815 6816 6817 6819
RE161	F	00008EB0	4	6872	6853 6854 6855 6857
RE162	F	00008F78	4	6910	6891 6892 6893 6895
RE163	F	00009040	4	6948	6929 6930 6931 6933
RE164	F	00009108	4	6986	6967 6968 6969 6971
RE165	F	000091D0	4	7024	7005 7006 7007 7009
RE166	F	00009298	4	7062	7043 7044 7045 7047
RE167	F	00009360	4	7101	7082 7083 7084 7086
RE168	F	00009428	4	7139	7120 7121 7122 7124
RE169	F	000094F0	4	7177	7158 7159 7160 7162
RE17	F	00001E30	4	1318	1299 1300 1301 1303
RE170	F	000095B8	4	7215	7196 7197 7198 7200
RE171	F	00009680	4	7253	7234 7235 7236 7238
RE172	F	00009748	4	7291	7272 7273 7274 7276
RE173	F	00009810	4	7329	7310 7311 7312 7314
RE174	F	000098D8	4	7367	7348 7349 7350 7352
RE175	F	000099A0	4	7406	7387 7388 7389 7391
RE176	F	00009A68	4	7444	7425 7426 7427 7429
RE177	F	00009B30	4	7482	7463 7464 7465 7467
RE178	F	00009BF8	4	7520	7501 7502 7503 7505
RE179	F	00009CC0	4	7558	7539 7540 7541 7543
RE18	F	00001EF8	4	1356	1337 1338 1339 1341
RE180	F	00009D88	4	7596	7577 7578 7579 7581
RE181	F	00009E50	4	7634	7615 7616 7617 7619
RE182	F	00009F18	4	7672	7653 7654 7655 7657
RE19	F	00001FC0	4	1394	1375 1376 1377 1379
RE2	F	00001278	4	741	722 723 724 726
RE20	F	00002088	4	1432	1413 1414 1415 1417
RE21	F	00002150	4	1470	1451 1452 1453 1455
RE22	F	00002218	4	1509	1490 1491 1492 1494
RE23	F	000022E0	4	1547	1528 1529 1530 1532
RE24	F	000023A8	4	1585	1566 1567 1568 1570
RE25	F	00002470	4	1623	1604 1605 1606 1608
RE26	F	00002538	4	1661	1642 1643 1644 1646
RE27	F	00002600	4	1699	1680 1681 1682 1684
RE28	F	000026C8	4	1739	1720 1721 1722 1724
RE29	F	00002790	4	1777	1758 1759 1760 1762
RE3	F	00001340	4	779	760 761 762 764
RE30	F	00002858	4	1815	1796 1797 1798 1800
RE31	F	00002920	4	1863	1844 1845 1846 1848
RE32	F	000029E8	4	1901	1882 1883 1884 1886
RE33	F	00002AB0	4	1939	1920 1921 1922 1924
RE34	F	00002B78	4	1978	1959 1960 1961 1963
RE35	F	00002C40	4	2016	1997 1998 1999 2001

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE36	F	00002D08	4	2054	2035 2036 2037 2039
RE37	F	00002DD0	4	2093	2074 2075 2076 2078
RE38	F	00002E98	4	2131	2112 2113 2114 2116
RE39	F	00002F60	4	2169	2150 2151 2152 2154
RE4	F	00001408	4	818	799 800 801 803
RE40	F	00003028	4	2211	2192 2193 2194 2196
RE41	F	000030F0	4	2249	2230 2231 2232 2234
RE42	F	000031B8	4	2287	2268 2269 2270 2272
RE43	F	00003280	4	2325	2306 2307 2308 2310
RE44	F	00003348	4	2363	2344 2345 2346 2348
RE45	F	00003410	4	2401	2382 2383 2384 2386
RE46	F	000034D8	4	2439	2420 2421 2422 2424
RE47	F	000035A0	4	2477	2458 2459 2460 2462
RE48	F	00003668	4	2516	2497 2498 2499 2501
RE49	F	00003730	4	2554	2535 2536 2537 2539
RE5	F	000014D0	4	856	837 838 839 841
RE50	F	000037F8	4	2592	2573 2574 2575 2577
RE51	F	000038C0	4	2630	2611 2612 2613 2615
RE52	F	00003988	4	2668	2649 2650 2651 2653
RE53	F	00003A50	4	2706	2687 2688 2689 2691
RE54	F	00003B18	4	2744	2725 2726 2727 2729
RE55	F	00003BE0	4	2782	2763 2764 2765 2767
RE56	F	00003CA8	4	2821	2802 2803 2804 2806
RE57	F	00003D70	4	2859	2840 2841 2842 2844
RE58	F	00003E38	4	2897	2878 2879 2880 2882
RE59	F	00003F00	4	2935	2916 2917 2918 2920
RE6	F	00001598	4	894	875 876 877 879
RE60	F	00003FC8	4	2973	2954 2955 2956 2958
RE61	F	00004090	4	3011	2992 2993 2994 2996
RE62	F	00004158	4	3049	3030 3031 3032 3034
RE63	F	00004220	4	3087	3068 3069 3070 3072
RE64	F	000042E8	4	3128	3109 3110 3111 3113
RE65	F	000043B0	4	3166	3147 3148 3149 3151
RE66	F	00004478	4	3204	3185 3186 3187 3189
RE67	F	00004540	4	3252	3233 3234 3235 3237
RE68	F	00004608	4	3290	3271 3272 3273 3275
RE69	F	000046D0	4	3328	3309 3310 3311 3313
RE7	F	00001660	4	933	914 915 916 918
RE70	F	00004798	4	3367	3348 3349 3350 3352
RE71	F	00004860	4	3405	3386 3387 3388 3390
RE72	F	00004928	4	3443	3424 3425 3426 3428
RE73	F	000049F0	4	3482	3463 3464 3465 3467
RE74	F	00004AB8	4	3520	3501 3502 3503 3505
RE75	F	00004B80	4	3558	3539 3540 3541 3543
RE76	F	00004C48	4	3597	3578 3579 3580 3582
RE77	F	00004D10	4	3635	3616 3617 3618 3620
RE78	F	00004DD8	4	3673	3654 3655 3656 3658
RE79	F	00004EA0	4	3715	3696 3697 3698 3700
RE8	F	00001728	4	971	952 953 954 956
RE80	F	00004F68	4	3753	3734 3735 3736 3738
RE81	F	00005030	4	3791	3772 3773 3774 3776
RE82	F	000050F8	4	3829	3810 3811 3812 3814
RE83	F	000051C0	4	3867	3848 3849 3850 3852
RE84	F	00005288	4	3905	3886 3887 3888 3890
RE85	F	00005350	4	3944	3925 3926 3927 3929
RE86	F	00005418	4	3982	3963 3964 3965 3967

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
RE87	F	000054E0	4	4020	4001	4002	4003	4005	
RE88	F	000055A8	4	4058	4039	4040	4041	4043	
RE89	F	00005670	4	4096	4077	4078	4079	4081	
RE9	F	000017F0	4	1009	990	991	992	994	
RE90	F	00005738	4	4134	4115	4116	4117	4119	
RE91	F	00005800	4	4173	4154	4155	4156	4158	
RE92	F	000058C8	4	4211	4192	4193	4194	4196	
RE93	F	00005990	4	4249	4230	4231	4232	4234	
RE94	F	00005A58	4	4287	4268	4269	4270	4272	
RE95	F	00005B20	4	4325	4306	4307	4308	4310	
RE96	F	00005BE8	4	4363	4344	4345	4346	4348	
RE97	F	00005CB0	4	4402	4383	4384	4385	4387	
RE98	F	00005D78	4	4440	4421	4422	4423	4425	
RE99	F	00005E40	4	4478	4459	4460	4461	4463	
REA1	A	00001148	4	688					
REA10	A	00001850	4	1036					
REA100	A	00005EA0	4	4501					
REA101	A	00005F68	4	4539					
REA102	A	00006030	4	4577					
REA103	A	000060F8	4	4625					
REA104	A	000061C0	4	4663					
REA105	A	00006288	4	4701					
REA106	A	00006350	4	4740					
REA107	A	00006418	4	4778					
REA108	A	000064E0	4	4816					
REA109	A	000065A8	4	4855					
REA11	A	00001918	4	1074					
REA110	A	00006670	4	4893					
REA111	A	00006738	4	4931					
REA112	A	00006800	4	4970					
REA113	A	000068C8	4	5008					
REA114	A	00006990	4	5046					
REA115	A	00006A58	4	5088					
REA116	A	00006B20	4	5126					
REA117	A	00006BE8	4	5164					
REA118	A	00006CB0	4	5202					
REA119	A	00006D78	4	5240					
REA12	A	000019E0	4	1112					
REA120	A	00006E40	4	5278					
REA121	A	00006F08	4	5317					
REA122	A	00006FD0	4	5355					
REA123	A	00007098	4	5393					
REA124	A	00007160	4	5431					
REA125	A	00007228	4	5469					
REA126	A	000072F0	4	5507					
REA127	A	000073B8	4	5546					
REA128	A	00007480	4	5584					
REA129	A	00007548	4	5622					
REA13	A	00001AA8	4	1150					
REA130	A	00007610	4	5660					
REA131	A	000076D8	4	5698					
REA132	A	000077A0	4	5736					
REA133	A	00007868	4	5775					
REA134	A	00007930	4	5813					
REA135	A	000079F8	4	5851					
REA136	A	00007AC0	4	5889					

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA137	A	00007B88	4	5927	
REA138	A	00007C50	4	5965	
REA139	A	00007D18	4	6013	
REA14	A	00001B70	4	1188	
REA140	A	00007DE0	4	6051	
REA141	A	00007EA8	4	6089	
REA142	A	00007F70	4	6128	
REA143	A	00008038	4	6166	
REA144	A	00008100	4	6204	
REA145	A	000081C8	4	6243	
REA146	A	00008290	4	6281	
REA147	A	00008358	4	6319	
REA148	A	00008420	4	6358	
REA149	A	000084E8	4	6396	
REA15	A	00001C38	4	1226	
REA150	A	000085B0	4	6434	
REA151	A	00008678	4	6476	
REA152	A	00008740	4	6514	
REA153	A	00008808	4	6552	
REA154	A	000088D0	4	6590	
REA155	A	00008998	4	6628	
REA156	A	00008A60	4	6666	
REA157	A	00008B28	4	6704	
REA158	A	00008BF0	4	6742	
REA159	A	00008CB8	4	6781	
REA16	A	00001D00	4	1265	
REA160	A	00008D80	4	6819	
REA161	A	00008E48	4	6857	
REA162	A	00008F10	4	6895	
REA163	A	00008FD8	4	6933	
REA164	A	000090A0	4	6971	
REA165	A	00009168	4	7009	
REA166	A	00009230	4	7047	
REA167	A	000092F8	4	7086	
REA168	A	000093C0	4	7124	
REA169	A	00009488	4	7162	
REA17	A	00001DC8	4	1303	
REA170	A	00009550	4	7200	
REA171	A	00009618	4	7238	
REA172	A	000096E0	4	7276	
REA173	A	000097A8	4	7314	
REA174	A	00009870	4	7352	
REA175	A	00009938	4	7391	
REA176	A	00009A00	4	7429	
REA177	A	00009AC8	4	7467	
REA178	A	00009B90	4	7505	
REA179	A	00009C58	4	7543	
REA18	A	00001E90	4	1341	
REA180	A	00009D20	4	7581	
REA181	A	00009DE8	4	7619	
REA182	A	00009EB0	4	7657	
REA19	A	00001F58	4	1379	
REA2	A	00001210	4	726	
REA20	A	00002020	4	1417	
REA21	A	000020E8	4	1455	
REA22	A	000021B0	4	1494	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA23	A	00002278	4	1532	
REA24	A	00002340	4	1570	
REA25	A	00002408	4	1608	
REA26	A	000024D0	4	1646	
REA27	A	00002598	4	1684	
REA28	A	00002660	4	1724	
REA29	A	00002728	4	1762	
REA3	A	000012D8	4	764	
REA30	A	000027F0	4	1800	
REA31	A	000028B8	4	1848	
REA32	A	00002980	4	1886	
REA33	A	00002A48	4	1924	
REA34	A	00002B10	4	1963	
REA35	A	00002BD8	4	2001	
REA36	A	00002CA0	4	2039	
REA37	A	00002D68	4	2078	
REA38	A	00002E30	4	2116	
REA39	A	00002EF8	4	2154	
REA4	A	000013A0	4	803	
REA40	A	00002FC0	4	2196	
REA41	A	00003088	4	2234	
REA42	A	00003150	4	2272	
REA43	A	00003218	4	2310	
REA44	A	000032E0	4	2348	
REA45	A	000033A8	4	2386	
REA46	A	00003470	4	2424	
REA47	A	00003538	4	2462	
REA48	A	00003600	4	2501	
REA49	A	000036C8	4	2539	
REA5	A	00001468	4	841	
REA50	A	00003790	4	2577	
REA51	A	00003858	4	2615	
REA52	A	00003920	4	2653	
REA53	A	000039E8	4	2691	
REA54	A	00003AB0	4	2729	
REA55	A	00003B78	4	2767	
REA56	A	00003C40	4	2806	
REA57	A	00003D08	4	2844	
REA58	A	00003DD0	4	2882	
REA59	A	00003E98	4	2920	
REA6	A	00001530	4	879	
REA60	A	00003F60	4	2958	
REA61	A	00004028	4	2996	
REA62	A	000040F0	4	3034	
REA63	A	000041B8	4	3072	
REA64	A	00004280	4	3113	
REA65	A	00004348	4	3151	
REA66	A	00004410	4	3189	
REA67	A	000044D8	4	3237	
REA68	A	000045A0	4	3275	
REA69	A	00004668	4	3313	
REA7	A	000015F8	4	918	
REA70	A	00004730	4	3352	
REA71	A	000047F8	4	3390	
REA72	A	000048C0	4	3428	
REA73	A	00004988	4	3467	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA74	A	00004A50	4	3505		
REA75	A	00004B18	4	3543		
REA76	A	00004BE0	4	3582		
REA77	A	00004CA8	4	3620		
REA78	A	00004D70	4	3658		
REA79	A	00004E38	4	3700		
REA8	A	000016C0	4	956		
REA80	A	00004F00	4	3738		
REA81	A	00004FC8	4	3776		
REA82	A	00005090	4	3814		
REA83	A	00005158	4	3852		
REA84	A	00005220	4	3890		
REA85	A	000052E8	4	3929		
REA86	A	000053B0	4	3967		
REA87	A	00005478	4	4005		
REA88	A	00005540	4	4043		
REA89	A	00005608	4	4081		
REA9	A	00001788	4	994		
REA90	A	000056D0	4	4119		
REA91	A	00005798	4	4158		
REA92	A	00005860	4	4196		
REA93	A	00005928	4	4234		
REA94	A	000059F0	4	4272		
REA95	A	00005AB8	4	4310		
REA96	A	00005B80	4	4348		
REA97	A	00005C48	4	4387		
REA98	A	00005D10	4	4425		
REA99	A	00005DD8	4	4463		
READDR	A	00000030	4	535	234	
REG2LOW	U	000000DD	1	445		
REG2PATT	U	AABBCCDD	1	444		
RELEN	A	0000002C	4	534		
RPTDWSAV	D	00000460	8	368	357	359
RPTERROR	I	00000436	4	352	287	325
RPTSAVE	F	00000454	4	365	352	362
RPTSVR5	F	00000458	4	366	353	361
SKL0001	U	0000004E	1	187	203	
SKT0001	C	0000022A	20	184	187	204
SVOLDPSW	U	00000140	0	123		
T1	A	00001118	4	674	7688	
T10	A	00001820	4	1022	7697	
T100	A	00005E70	4	4487	7787	
T101	A	00005F38	4	4525	7788	
T102	A	00006000	4	4563	7789	
T103	A	000060C8	4	4611	7790	
T104	A	00006190	4	4649	7791	
T105	A	00006258	4	4687	7792	
T106	A	00006320	4	4726	7793	
T107	A	000063E8	4	4764	7794	
T108	A	000064B0	4	4802	7795	
T109	A	00006578	4	4841	7796	
T11	A	000018E8	4	1060	7698	
T110	A	00006640	4	4879	7797	
T111	A	00006708	4	4917	7798	
T112	A	000067D0	4	4956	7799	
T113	A	00006898	4	4994	7800	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T114	A	00006960	4	5032	7801
T115	A	00006A28	4	5074	7802
T116	A	00006AF0	4	5112	7803
T117	A	00006BB8	4	5150	7804
T118	A	00006C80	4	5188	7805
T119	A	00006D48	4	5226	7806
T12	A	000019B0	4	1098	7699
T120	A	00006E10	4	5264	7807
T121	A	00006ED8	4	5303	7808
T122	A	00006FA0	4	5341	7809
T123	A	00007068	4	5379	7810
T124	A	00007130	4	5417	7811
T125	A	000071F8	4	5455	7812
T126	A	000072C0	4	5493	7813
T127	A	00007388	4	5532	7814
T128	A	00007450	4	5570	7815
T129	A	00007518	4	5608	7816
T13	A	00001A78	4	1136	7700
T130	A	000075E0	4	5646	7817
T131	A	000076A8	4	5684	7818
T132	A	00007770	4	5722	7819
T133	A	00007838	4	5761	7820
T134	A	00007900	4	5799	7821
T135	A	000079C8	4	5837	7822
T136	A	00007A90	4	5875	7823
T137	A	00007B58	4	5913	7824
T138	A	00007C20	4	5951	7825
T139	A	00007CE8	4	5999	7826
T14	A	00001B40	4	1174	7701
T140	A	00007DB0	4	6037	7827
T141	A	00007E78	4	6075	7828
T142	A	00007F40	4	6114	7829
T143	A	00008008	4	6152	7830
T144	A	000080D0	4	6190	7831
T145	A	00008198	4	6229	7832
T146	A	00008260	4	6267	7833
T147	A	00008328	4	6305	7834
T148	A	000083F0	4	6344	7835
T149	A	000084B8	4	6382	7836
T15	A	00001C08	4	1212	7702
T150	A	00008580	4	6420	7837
T151	A	00008648	4	6462	7838
T152	A	00008710	4	6500	7839
T153	A	000087D8	4	6538	7840
T154	A	000088A0	4	6576	7841
T155	A	00008968	4	6614	7842
T156	A	00008A30	4	6652	7843
T157	A	00008AF8	4	6690	7844
T158	A	00008BC0	4	6728	7845
T159	A	00008C88	4	6767	7846
T16	A	00001CD0	4	1251	7703
T160	A	00008D50	4	6805	7847
T161	A	00008E18	4	6843	7848
T162	A	00008EE0	4	6881	7849
T163	A	00008FA8	4	6919	7850
T164	A	00009070	4	6957	7851

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T165	A	00009138	4	6995	7852
T166	A	00009200	4	7033	7853
T167	A	000092C8	4	7072	7854
T168	A	00009390	4	7110	7855
T169	A	00009458	4	7148	7856
T17	A	00001D98	4	1289	7704
T170	A	00009520	4	7186	7857
T171	A	000095E8	4	7224	7858
T172	A	000096B0	4	7262	7859
T173	A	00009778	4	7300	7860
T174	A	00009840	4	7338	7861
T175	A	00009908	4	7377	7862
T176	A	000099D0	4	7415	7863
T177	A	00009A98	4	7453	7864
T178	A	00009B60	4	7491	7865
T179	A	00009C28	4	7529	7866
T18	A	00001E60	4	1327	7705
T180	A	00009CF0	4	7567	7867
T181	A	00009DB8	4	7605	7868
T182	A	00009E80	4	7643	7869
T19	A	00001F28	4	1365	7706
T2	A	000011E0	4	712	7689
T20	A	00001FF0	4	1403	7707
T21	A	000020B8	4	1441	7708
T22	A	00002180	4	1480	7709
T23	A	00002248	4	1518	7710
T24	A	00002310	4	1556	7711
T25	A	000023D8	4	1594	7712
T26	A	000024A0	4	1632	7713
T27	A	00002568	4	1670	7714
T28	A	00002630	4	1710	7715
T29	A	000026F8	4	1748	7716
T3	A	000012A8	4	750	7690
T30	A	000027C0	4	1786	7717
T31	A	00002888	4	1834	7718
T32	A	00002950	4	1872	7719
T33	A	00002A18	4	1910	7720
T34	A	00002AE0	4	1949	7721
T35	A	00002BA8	4	1987	7722
T36	A	00002C70	4	2025	7723
T37	A	00002D38	4	2064	7724
T38	A	00002E00	4	2102	7725
T39	A	00002EC8	4	2140	7726
T4	A	00001370	4	789	7691
T40	A	00002F90	4	2182	7727
T41	A	00003058	4	2220	7728
T42	A	00003120	4	2258	7729
T43	A	000031E8	4	2296	7730
T44	A	000032B0	4	2334	7731
T45	A	00003378	4	2372	7732
T46	A	00003440	4	2410	7733
T47	A	00003508	4	2448	7734
T48	A	000035D0	4	2487	7735
T49	A	00003698	4	2525	7736
T5	A	00001438	4	827	7692
T50	A	00003760	4	2563	7737

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T51	A	00003828	4	2601	7738
T52	A	000038F0	4	2639	7739
T53	A	000039B8	4	2677	7740
T54	A	00003A80	4	2715	7741
T55	A	00003B48	4	2753	7742
T56	A	00003C10	4	2792	7743
T57	A	00003CD8	4	2830	7744
T58	A	00003DA0	4	2868	7745
T59	A	00003E68	4	2906	7746
T6	A	00001500	4	865	7693
T60	A	00003F30	4	2944	7747
T61	A	00003FF8	4	2982	7748
T62	A	000040C0	4	3020	7749
T63	A	00004188	4	3058	7750
T64	A	00004250	4	3099	7751
T65	A	00004318	4	3137	7752
T66	A	000043E0	4	3175	7753
T67	A	000044A8	4	3223	7754
T68	A	00004570	4	3261	7755
T69	A	00004638	4	3299	7756
T7	A	000015C8	4	904	7694
T70	A	00004700	4	3338	7757
T71	A	000047C8	4	3376	7758
T72	A	00004890	4	3414	7759
T73	A	00004958	4	3453	7760
T74	A	00004A20	4	3491	7761
T75	A	00004AE8	4	3529	7762
T76	A	00004BB0	4	3568	7763
T77	A	00004C78	4	3606	7764
T78	A	00004D40	4	3644	7765
T79	A	00004E08	4	3686	7766
T8	A	00001690	4	942	7695
T80	A	00004ED0	4	3724	7767
T81	A	00004F98	4	3762	7768
T82	A	00005060	4	3800	7769
T83	A	00005128	4	3838	7770
T84	A	000051F0	4	3876	7771
T85	A	000052B8	4	3915	7772
T86	A	00005380	4	3953	7773
T87	A	00005448	4	3991	7774
T88	A	00005510	4	4029	7775
T89	A	000055D8	4	4067	7776
T9	A	00001758	4	980	7696
T90	A	000056A0	4	4105	7777
T91	A	00005768	4	4144	7778
T92	A	00005830	4	4182	7779
T93	A	000058F8	4	4220	7780
T94	A	000059C0	4	4258	7781
T95	A	00005A88	4	4296	7782
T96	A	00005B50	4	4334	7783
T97	A	00005C18	4	4373	7784
T98	A	00005CE0	4	4411	7785
T99	A	00005DA8	4	4449	7786
TESTCC	I	00000318	4	241	231
TESTING	F	00001004	4	456	223
TESTREST	U	00000300	1	233	252 292

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
TNUM	H	00000004	2	518	222	263	301
TSUB	A	00000000	4	517	226		
TTABLE	F	00009F50	4	7687			
V0	U	00000000	1	7902			
V1	U	00000001	1	7903			
V10	U	0000000A	1	7912			
V11	U	0000000B	1	7913			
V12	U	0000000C	1	7914			
V13	U	0000000D	1	7915			
V14	U	0000000E	1	7916			
V15	U	0000000F	1	7917			
V16	U	00000010	1	7918			
V17	U	00000011	1	7919			
V18	U	00000012	1	7920			
V19	U	00000013	1	7921			
V1ADDR	A	00000020	4	531			
V1FUDGE	X	000010F8	16	509	225		
V101	X	00001160	16	690	701		
V1010	X	00001868	16	1038	1049		
V10100	X	00005EB8	16	4503	4514		
V10101	X	00005F80	16	4541	4552		
V10102	X	00006048	16	4579	4590		
V10103	X	00006110	16	4627	4638		
V10104	X	000061D8	16	4665	4676		
V10105	X	000062A0	16	4703	4714		
V10106	X	00006368	16	4742	4753		
V10107	X	00006430	16	4780	4791		
V10108	X	000064F8	16	4818	4829		
V10109	X	000065C0	16	4857	4868		
V1011	X	00001930	16	1076	1087		
V10110	X	00006688	16	4895	4906		
V10111	X	00006750	16	4933	4944		
V10112	X	00006818	16	4972	4983		
V10113	X	000068E0	16	5010	5021		
V10114	X	000069A8	16	5048	5059		
V10115	X	00006A70	16	5090	5101		
V10116	X	00006B38	16	5128	5139		
V10117	X	00006C00	16	5166	5177		
V10118	X	00006CC8	16	5204	5215		
V10119	X	00006D90	16	5242	5253		
V1012	X	000019F8	16	1114	1125		
V10120	X	00006E58	16	5280	5291		
V10121	X	00006F20	16	5319	5330		
V10122	X	00006FE8	16	5357	5368		
V10123	X	000070B0	16	5395	5406		
V10124	X	00007178	16	5433	5444		
V10125	X	00007240	16	5471	5482		
V10126	X	00007308	16	5509	5520		
V10127	X	000073D0	16	5548	5559		
V10128	X	00007498	16	5586	5597		
V10129	X	00007560	16	5624	5635		
V1013	X	00001AC0	16	1152	1163		
V10130	X	00007628	16	5662	5673		
V10131	X	000076F0	16	5700	5711		
V10132	X	000077B8	16	5738	5749		
V10133	X	00007880	16	5777	5788		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10134	X	00007948	16	5815	5826
V10135	X	00007A10	16	5853	5864
V10136	X	00007AD8	16	5891	5902
V10137	X	00007BA0	16	5929	5940
V10138	X	00007C68	16	5967	5978
V10139	X	00007D30	16	6015	6026
V1014	X	00001B88	16	1190	1201
V10140	X	00007DF8	16	6053	6064
V10141	X	00007EC0	16	6091	6102
V10142	X	00007F88	16	6130	6141
V10143	X	00008050	16	6168	6179
V10144	X	00008118	16	6206	6217
V10145	X	000081E0	16	6245	6256
V10146	X	000082A8	16	6283	6294
V10147	X	00008370	16	6321	6332
V10148	X	00008438	16	6360	6371
V10149	X	00008500	16	6398	6409
V1015	X	00001C50	16	1228	1239
V10150	X	000085C8	16	6436	6447
V10151	X	00008690	16	6478	6489
V10152	X	00008758	16	6516	6527
V10153	X	00008820	16	6554	6565
V10154	X	000088E8	16	6592	6603
V10155	X	000089B0	16	6630	6641
V10156	X	00008A78	16	6668	6679
V10157	X	00008B40	16	6706	6717
V10158	X	00008C08	16	6744	6755
V10159	X	00008CD0	16	6783	6794
V1016	X	00001D18	16	1267	1278
V10160	X	00008D98	16	6821	6832
V10161	X	00008E60	16	6859	6870
V10162	X	00008F28	16	6897	6908
V10163	X	00008FF0	16	6935	6946
V10164	X	000090B8	16	6973	6984
V10165	X	00009180	16	7011	7022
V10166	X	00009248	16	7049	7060
V10167	X	00009310	16	7088	7099
V10168	X	000093D8	16	7126	7137
V10169	X	000094A0	16	7164	7175
V1017	X	00001DE0	16	1305	1316
V10170	X	00009568	16	7202	7213
V10171	X	00009630	16	7240	7251
V10172	X	000096F8	16	7278	7289
V10173	X	000097C0	16	7316	7327
V10174	X	00009888	16	7354	7365
V10175	X	00009950	16	7393	7404
V10176	X	00009A18	16	7431	7442
V10177	X	00009AE0	16	7469	7480
V10178	X	00009BA8	16	7507	7518
V10179	X	00009C70	16	7545	7556
V1018	X	00001EA8	16	1343	1354
V10180	X	00009D38	16	7583	7594
V10181	X	00009E00	16	7621	7632
V10182	X	00009EC8	16	7659	7670
V1019	X	00001F70	16	1381	1392
V102	X	00001228	16	728	739

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1020	X	00002038	16	1419	1430
V1021	X	00002100	16	1457	1468
V1022	X	000021C8	16	1496	1507
V1023	X	00002290	16	1534	1545
V1024	X	00002358	16	1572	1583
V1025	X	00002420	16	1610	1621
V1026	X	000024E8	16	1648	1659
V1027	X	000025B0	16	1686	1697
V1028	X	00002678	16	1726	1737
V1029	X	00002740	16	1764	1775
V103	X	000012F0	16	766	777
V1030	X	00002808	16	1802	1813
V1031	X	000028D0	16	1850	1861
V1032	X	00002998	16	1888	1899
V1033	X	00002A60	16	1926	1937
V1034	X	00002B28	16	1965	1976
V1035	X	00002BF0	16	2003	2014
V1036	X	00002CB8	16	2041	2052
V1037	X	00002D80	16	2080	2091
V1038	X	00002E48	16	2118	2129
V1039	X	00002F10	16	2156	2167
V104	X	000013B8	16	805	816
V1040	X	00002FD8	16	2198	2209
V1041	X	000030A0	16	2236	2247
V1042	X	00003168	16	2274	2285
V1043	X	00003230	16	2312	2323
V1044	X	000032F8	16	2350	2361
V1045	X	000033C0	16	2388	2399
V1046	X	00003488	16	2426	2437
V1047	X	00003550	16	2464	2475
V1048	X	00003618	16	2503	2514
V1049	X	000036E0	16	2541	2552
V105	X	00001480	16	843	854
V1050	X	000037A8	16	2579	2590
V1051	X	00003870	16	2617	2628
V1052	X	00003938	16	2655	2666
V1053	X	00003A00	16	2693	2704
V1054	X	00003AC8	16	2731	2742
V1055	X	00003B90	16	2769	2780
V1056	X	00003C58	16	2808	2819
V1057	X	00003D20	16	2846	2857
V1058	X	00003DE8	16	2884	2895
V1059	X	00003EB0	16	2922	2933
V106	X	00001548	16	881	892
V1060	X	00003F78	16	2960	2971
V1061	X	00004040	16	2998	3009
V1062	X	00004108	16	3036	3047
V1063	X	000041D0	16	3074	3085
V1064	X	00004298	16	3115	3126
V1065	X	00004360	16	3153	3164
V1066	X	00004428	16	3191	3202
V1067	X	000044F0	16	3239	3250
V1068	X	000045B8	16	3277	3288
V1069	X	00004680	16	3315	3326
V107	X	00001610	16	920	931
V1070	X	00004748	16	3354	3365

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1071	X	00004810	16	3392	3403												
V1072	X	000048D8	16	3430	3441												
V1073	X	000049A0	16	3469	3480												
V1074	X	00004A68	16	3507	3518												
V1075	X	00004B30	16	3545	3556												
V1076	X	00004BF8	16	3584	3595												
V1077	X	00004CC0	16	3622	3633												
V1078	X	00004D88	16	3660	3671												
V1079	X	00004E50	16	3702	3713												
V108	X	000016D8	16	958	969												
V1080	X	00004F18	16	3740	3751												
V1081	X	00004FE0	16	3778	3789												
V1082	X	000050A8	16	3816	3827												
V1083	X	00005170	16	3854	3865												
V1084	X	00005238	16	3892	3903												
V1085	X	00005300	16	3931	3942												
V1086	X	000053C8	16	3969	3980												
V1087	X	00005490	16	4007	4018												
V1088	X	00005558	16	4045	4056												
V1089	X	00005620	16	4083	4094												
V109	X	000017A0	16	996	1007												
V1090	X	000056E8	16	4121	4132												
V1091	X	000057B0	16	4160	4171												
V1092	X	00005878	16	4198	4209												
V1093	X	00005940	16	4236	4247												
V1094	X	00005A08	16	4274	4285												
V1095	X	00005AD0	16	4312	4323												
V1096	X	00005B98	16	4350	4361												
V1097	X	00005C60	16	4389	4400												
V1098	X	00005D28	16	4427	4438												
V1099	X	00005DF0	16	4465	4476												
V10UTPUT	X	00000048	16	537	235												
V2	U	00000002	1	7904													
V20	U	00000014	1	7922													
V21	U	00000015	1	7923	698	701	736	739	774	777	813	816	851	854	889	892	928
					931	966	969	1004	1007	1046	1049	1084	1087	1122	1125	1160	1163
					1198	1201	1236	1239	1275	1278	1313	1316	1351	1354	1389	1392	1427
					1430	1465	1468	1504	1507	1542	1545	1580	1583	1618	1621	1656	1659
					1694	1697	1734	1737	1772	1775	1810	1813	1858	1861	1896	1899	1934
					1937	1973	1976	2011	2014	2049	2052	2088	2091	2126	2129	2164	2167
					2206	2209	2244	2247	2282	2285	2320	2323	2358	2361	2396	2399	2434
					2437	2472	2475	2511	2514	2549	2552	2587	2590	2625	2628	2663	2666
					2701	2704	2739	2742	2777	2780	2816	2819	2854	2857	2892	2895	2930
					2933	2968	2971	3006	3009	3044	3047	3082	3085	3123	3126	3161	3164
					3199	3202	3247	3250	3285	3288	3323	3326	3362	3365	3400	3403	3438
					3441	3477	3480	3515	3518	3553	3556	3592	3595	3630	3633	3668	3671
					3710	3713	3748	3751	3786	3789	3824	3827	3862	3865	3900	3903	3939
					3942	3977	3980	4015	4018	4053	4056	4091	4094	4129	4132	4168	4171
					4206	4209	4244	4247	4282	4285	4320	4323	4358	4361	4397	4400	4435
					4438	4473	4476	4511	4514	4549	4552	4587	4590	4635	4638	4673	4676
					4711	4714	4750	4753	4788	4791	4826	4829	4865	4868	4903	4906	4941
					4944	4980	4983	5018	5021	5056	5059	5098	5101	5136	5139	5174	5177
					5212	5215	5250	5253	5288	5291	5327	5330	5365	5368	5403	5406	5441
					5444	5479	5482	5517	5520	5556	5559	5594	5597	5632	5635	5670	5673
					5708	5711	5746	5749	5785	5788	5823	5826	5861	5864	5899	5902	5937
					5940	5975	5978	6023	6026	6061	6064	6099	6102	6138	6141	6176	6179

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V22	U	00000016	1	7924	6214	6217	6253	6256	6291	6294	6329	6332	6368	6371	6406	6409	6444
					6447	6486	6489	6524	6527	6562	6565	6600	6603	6638	6641	6676	6679
					6714	6717	6752	6755	6791	6794	6829	6832	6867	6870	6905	6908	6943
					6946	6981	6984	7019	7022	7057	7060	7096	7099	7134	7137	7172	7175
					7210	7213	7248	7251	7286	7289	7324	7327	7362	7365	7401	7404	7439
					7442	7477	7480	7515	7518	7553	7556	7591	7594	7629	7632	7667	7670
					225	695	698	733	736	771	774	810	813	848	851	886	889
					925	928	963	966	1001	1004	1043	1046	1081	1084	1119	1122	1157
					1160	1195	1198	1233	1236	1272	1275	1310	1313	1348	1351	1386	1389
					1424	1427	1462	1465	1501	1504	1539	1542	1577	1580	1615	1618	1653
					1656	1691	1694	1731	1734	1769	1772	1807	1810	1855	1858	1893	1896
					1931	1934	1970	1973	2008	2011	2046	2049	2085	2088	2123	2126	2161
					2164	2203	2206	2241	2244	2279	2282	2317	2320	2355	2358	2393	2396
					2431	2434	2469	2472	2508	2511	2546	2549	2584	2587	2622	2625	2660
					2663	2698	2701	2736	2739	2774	2777	2813	2816	2851	2854	2889	2892
					2927	2930	2965	2968	3003	3006	3041	3044	3079	3082	3120	3123	3158
					3161	3196	3199	3244	3247	3282	3285	3320	3323	3359	3362	3397	3400
					3435	3438	3474	3477	3512	3515	3550	3553	3589	3592	3627	3630	3665
					3668	3707	3710	3745	3748	3783	3786	3821	3824	3859	3862	3897	3900
					3936	3939	3974	3977	4012	4015	4050	4053	4088	4091	4126	4129	4165
					4168	4203	4206	4241	4244	4279	4282	4317	4320	4355	4358	4394	4397
					4432	4435	4470	4473	4508	4511	4546	4549	4584	4587	4632	4635	4670
					4673	4708	4711	4747	4750	4785	4788	4823	4826	4862	4865	4900	4903
					4938	4941	4977	4980	5015	5018	5053	5056	5095	5098	5133	5136	5171
					5174	5209	5212	5247	5250	5285	5288	5324	5327	5362	5365	5400	5403
					5438	5441	5476	5479	5514	5517	5553	5556	5591	5594	5629	5632	5667
					5670	5705	5708	5743	5746	5782	5785	5820	5823	5858	5861	5896	5899
					5934	5937	5972	5975	6020	6023	6058	6061	6096	6099	6135	6138	6173
					6176	6211	6214	6250	6253	6288	6291	6326	6329	6365	6368	6403	6406
V23	U	00000017	1	7925	6441	6444	6483	6486	6521	6524	6559	6562	6597	6600	6635	6638	6673
					6676	6711	6714	6749	6752	6788	6791	6826	6829	6864	6867	6902	6905
					6940	6943	6978	6981	7016	7019	7054	7057	7093	7096	7131	7134	7169
					7172	7207	7210	7245	7248	7283	7286	7321	7324	7359	7362	7398	7401
					7436	7439	7474	7477	7512	7515	7550	7553	7588	7591	7626	7629	7664
					7667	697	698	735	736	773	774	812	813	850	851	888	889
					928	965	966	1003	1004	1045	1046	1083	1084	1121	1122	1159	1160
					1197	1198	1235	1236	1274	1275	1312	1313	1350	1351	1388	1389	1426
					1427	1464	1465	1503	1504	1541	1542	1579	1580	1617	1618	1655	1656
					1693	1694	1733	1734	1771	1772	1809	1810	1857	1858	1895	1896	1933
					1934	1972	1973	2010	2011	2048	2049	2087	2088	2125	2126	2163	2164
					2205	2206	2243	2244	2281	2282	2319	2320	2357	2358	2395	2396	2433
					2434	2471	2472	2510	2511	2548	2549	2586	2587	2624	2625	2662	2663
					2700	2701	2738	2739	2776	2777	2815	2816	2853	2854	2891	2892	2929
					2930	2967	2968	3005	3006	3043	3044	3081	3082	3122	3123	3160	3161
					3198	3199	3246	3247	3284	3285	3322	3323	3361	3362	3399	3400	3437
					3438	3476	3477	3514	3515	3552	3553	3591	3592	3629	3630	3667	3668
					3709	3710	3747	3748	3785	3786	3823	3824	3861	3862	3899	3900	3938
					3939	3976	3977	4014	4015	4052	4053	4090	4091	4128	4129	4167	4168
					4205	4206	4243	4244	4281	4282	4319	4320	4357	4358	4396	4397	4434
					4435	4472	4473	4510	4511	4548	4549	4586	4587	4634	4635	4672	4673
					4710	4711	4749	4750	4787	4788	4825	4826	4864	4865	4902	4903	4940
					4941	4979	4980	5017	5018	5055	5056	5097	5098	5135	5136	5173	5174
					5211	5212	5249	5250	5287	5288	5326	5327	5364	5365	5402	5403	5440
					5441	5478	5479	5516	5517	5555	5556	5593	5594	5631	5632	5669	5670
					5707	5708	5745	5746	5784	5785	5822	5823	5860	5861	5898	5899	5936

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					5937	5974	5975	6022	6023	6060	6061	6098	6099	6137	6138	6175	6176
					6213	6214	6252	6253	6290	6291	6328	6329	6367	6368	6405	6406	6443
					6444	6485	6486	6523	6524	6561	6562	6599	6600	6637	6638	6675	6676
					6713	6714	6751	6752	6790	6791	6828	6829	6866	6867	6904	6905	6942
					6943	6980	6981	7018	7019	7056	7057	7095	7096	7133	7134	7171	7172
					7209	7210	7247	7248	7285	7286	7323	7324	7361	7362	7400	7401	7438
					7439	7476	7477	7514	7515	7552	7553	7590	7591	7628	7629	7666	7667
V24	U	00000018	1	7926													
V25	U	00000019	1	7927													
V26	U	0000001A	1	7928													
V27	U	0000001B	1	7929													
V28	U	0000001C	1	7930													
V29	U	0000001D	1	7931													
V2ADDR	A	00000024	4	532	694	732	770	809	847	885	924	962	1000	1042	1080	1118	1156
					1194	1232	1271	1309	1347	1385	1423	1461	1500	1538	1576	1614	1652
					1690	1730	1768	1806	1854	1892	1930	1969	2007	2045	2084	2122	2160
					2202	2240	2278	2316	2354	2392	2430	2468	2507	2545	2583	2621	2659
					2697	2735	2773	2812	2850	2888	2926	2964	3002	3040	3078	3119	3157
					3195	3243	3281	3319	3358	3396	3434	3473	3511	3549	3588	3626	3664
					3706	3744	3782	3820	3858	3896	3935	3973	4011	4049	4087	4125	4164
					4202	4240	4278	4316	4354	4393	4431	4469	4507	4545	4583	4631	4669
					4707	4746	4784	4822	4861	4899	4937	4976	5014	5052	5094	5132	5170
					5208	5246	5284	5323	5361	5399	5437	5475	5513	5552	5590	5628	5666
					5704	5742	5781	5819	5857	5895	5933	5971	6019	6057	6095	6134	6172
					6210	6249	6287	6325	6364	6402	6440	6482	6520	6558	6596	6634	6672
					6710	6748	6787	6825	6863	6901	6939	6977	7015	7053	7092	7130	7168
					7206	7244	7282	7320	7358	7397	7435	7473	7511	7549	7587	7625	7663
V3	U	00000003	1	7905													
V30	U	0000001E	1	7932													
V31	U	0000001F	1	7933													
V3ADDR	A	00000028	4	533	696	734	772	811	849	887	926	964	1002	1044	1082	1120	1158
					1196	1234	1273	1311	1349	1387	1425	1463	1502	1540	1578	1616	1654
					1692	1732	1770	1808	1856	1894	1932	1971	2009	2047	2086	2124	2162
					2204	2242	2280	2318	2356	2394	2432	2470	2509	2547	2585	2623	2661
					2699	2737	2775	2814	2852	2890	2928	2966	3004	3042	3080	3121	3159
					3197	3245	3283	3321	3360	3398	3436	3475	3513	3551	3590	3628	3666
					3708	3746	3784	3822	3860	3898	3937	3975	4013	4051	4089	4127	4166
					4204	4242	4280	4318	4356	4395	4433	4471	4509	4547	4585	4633	4671
					4709	4748	4786	4824	4863	4901	4939	4978	5016	5054	5096	5134	5172
					5210	5248	5286	5325	5363	5401	5439	5477	5515	5554	5592	5630	5668
					5706	5744	5783	5821	5859	5897	5935	5973	6021	6059	6097	6136	6174
					6212	6251	6289	6327	6366	6404	6442	6484	6522	6560	6598	6636	6674
					6712	6750	6789	6827	6865	6903	6941	6979	7017	7055	7094	7132	7170
					7208	7246	7284	7322	7360	7399	7437	7475	7513	7551	7589	7627	7665
V4	U	00000004	1	7906													
V5	U	00000005	1	7907													
V6	U	00000006	1	7908													
V7	U	00000007	1	7909													
V8	U	00000008	1	7910													
V9	U	00000009	1	7911													
X0001	U	000002A8	1	193	181	194											
X1	F	00001180	4	693	674												
X10	F	00001888	4	1041	1022												
X100	F	00005ED8	4	4506	4487												
X101	F	00005FA0	4	4544	4525												
X102	F	00006068	4	4582	4563												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X103	F	00006130	4	4630	4611
X104	F	000061F8	4	4668	4649
X105	F	000062C0	4	4706	4687
X106	F	00006388	4	4745	4726
X107	F	00006450	4	4783	4764
X108	F	00006518	4	4821	4802
X109	F	000065E0	4	4860	4841
X11	F	00001950	4	1079	1060
X110	F	000066A8	4	4898	4879
X111	F	00006770	4	4936	4917
X112	F	00006838	4	4975	4956
X113	F	00006900	4	5013	4994
X114	F	000069C8	4	5051	5032
X115	F	00006A90	4	5093	5074
X116	F	00006B58	4	5131	5112
X117	F	00006C20	4	5169	5150
X118	F	00006CE8	4	5207	5188
X119	F	00006DB0	4	5245	5226
X12	F	00001A18	4	1117	1098
X120	F	00006E78	4	5283	5264
X121	F	00006F40	4	5322	5303
X122	F	00007008	4	5360	5341
X123	F	000070D0	4	5398	5379
X124	F	00007198	4	5436	5417
X125	F	00007260	4	5474	5455
X126	F	00007328	4	5512	5493
X127	F	000073F0	4	5551	5532
X128	F	000074B8	4	5589	5570
X129	F	00007580	4	5627	5608
X13	F	00001AE0	4	1155	1136
X130	F	00007648	4	5665	5646
X131	F	00007710	4	5703	5684
X132	F	000077D8	4	5741	5722
X133	F	000078A0	4	5780	5761
X134	F	00007968	4	5818	5799
X135	F	00007A30	4	5856	5837
X136	F	00007AF8	4	5894	5875
X137	F	00007BC0	4	5932	5913
X138	F	00007C88	4	5970	5951
X139	F	00007D50	4	6018	5999
X14	F	00001BA8	4	1193	1174
X140	F	00007E18	4	6056	6037
X141	F	00007EE0	4	6094	6075
X142	F	00007FA8	4	6133	6114
X143	F	00008070	4	6171	6152
X144	F	00008138	4	6209	6190
X145	F	00008200	4	6248	6229
X146	F	000082C8	4	6286	6267
X147	F	00008390	4	6324	6305
X148	F	00008458	4	6363	6344
X149	F	00008520	4	6401	6382
X15	F	00001C70	4	1231	1212
X150	F	000085E8	4	6439	6420
X151	F	000086B0	4	6481	6462
X152	F	00008778	4	6519	6500
X153	F	00008840	4	6557	6538

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X154	F	00008908	4	6595	6576
X155	F	000089D0	4	6633	6614
X156	F	00008A98	4	6671	6652
X157	F	00008B60	4	6709	6690
X158	F	00008C28	4	6747	6728
X159	F	00008CF0	4	6786	6767
X16	F	00001D38	4	1270	1251
X160	F	00008DB8	4	6824	6805
X161	F	00008E80	4	6862	6843
X162	F	00008F48	4	6900	6881
X163	F	00009010	4	6938	6919
X164	F	000090D8	4	6976	6957
X165	F	000091A0	4	7014	6995
X166	F	00009268	4	7052	7033
X167	F	00009330	4	7091	7072
X168	F	000093F8	4	7129	7110
X169	F	000094C0	4	7167	7148
X17	F	00001E00	4	1308	1289
X170	F	00009588	4	7205	7186
X171	F	00009650	4	7243	7224
X172	F	00009718	4	7281	7262
X173	F	000097E0	4	7319	7300
X174	F	000098A8	4	7357	7338
X175	F	00009970	4	7396	7377
X176	F	00009A38	4	7434	7415
X177	F	00009B00	4	7472	7453
X178	F	00009BC8	4	7510	7491
X179	F	00009C90	4	7548	7529
X18	F	00001EC8	4	1346	1327
X180	F	00009D58	4	7586	7567
X181	F	00009E20	4	7624	7605
X182	F	00009EE8	4	7662	7643
X19	F	00001F90	4	1384	1365
X2	F	00001248	4	731	712
X20	F	00002058	4	1422	1403
X21	F	00002120	4	1460	1441
X22	F	000021E8	4	1499	1480
X23	F	000022B0	4	1537	1518
X24	F	00002378	4	1575	1556
X25	F	00002440	4	1613	1594
X26	F	00002508	4	1651	1632
X27	F	000025D0	4	1689	1670
X28	F	00002698	4	1729	1710
X29	F	00002760	4	1767	1748
X3	F	00001310	4	769	750
X30	F	00002828	4	1805	1786
X31	F	000028F0	4	1853	1834
X32	F	000029B8	4	1891	1872
X33	F	00002A80	4	1929	1910
X34	F	00002B48	4	1968	1949
X35	F	00002C10	4	2006	1987
X36	F	00002CD8	4	2044	2025
X37	F	00002DA0	4	2083	2064
X38	F	00002E68	4	2121	2102
X39	F	00002F30	4	2159	2140
X4	F	000013D8	4	808	789

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X40	F	00002FF8	4	2201	2182
X41	F	000030C0	4	2239	2220
X42	F	00003188	4	2277	2258
X43	F	00003250	4	2315	2296
X44	F	00003318	4	2353	2334
X45	F	000033E0	4	2391	2372
X46	F	000034A8	4	2429	2410
X47	F	00003570	4	2467	2448
X48	F	00003638	4	2506	2487
X49	F	00003700	4	2544	2525
X5	F	000014A0	4	846	827
X50	F	000037C8	4	2582	2563
X51	F	00003890	4	2620	2601
X52	F	00003958	4	2658	2639
X53	F	00003A20	4	2696	2677
X54	F	00003AE8	4	2734	2715
X55	F	00003BB0	4	2772	2753
X56	F	00003C78	4	2811	2792
X57	F	00003D40	4	2849	2830
X58	F	00003E08	4	2887	2868
X59	F	00003ED0	4	2925	2906
X6	F	00001568	4	884	865
X60	F	00003F98	4	2963	2944
X61	F	00004060	4	3001	2982
X62	F	00004128	4	3039	3020
X63	F	000041F0	4	3077	3058
X64	F	000042B8	4	3118	3099
X65	F	00004380	4	3156	3137
X66	F	00004448	4	3194	3175
X67	F	00004510	4	3242	3223
X68	F	000045D8	4	3280	3261
X69	F	000046A0	4	3318	3299
X7	F	00001630	4	923	904
X70	F	00004768	4	3357	3338
X71	F	00004830	4	3395	3376
X72	F	000048F8	4	3433	3414
X73	F	000049C0	4	3472	3453
X74	F	00004A88	4	3510	3491
X75	F	00004B50	4	3548	3529
X76	F	00004C18	4	3587	3568
X77	F	00004CE0	4	3625	3606
X78	F	00004DA8	4	3663	3644
X79	F	00004E70	4	3705	3686
X8	F	000016F8	4	961	942
X80	F	00004F38	4	3743	3724
X81	F	00005000	4	3781	3762
X82	F	000050C8	4	3819	3800
X83	F	00005190	4	3857	3838
X84	F	00005258	4	3895	3876
X85	F	00005320	4	3934	3915
X86	F	000053E8	4	3972	3953
X87	F	000054B0	4	4010	3991
X88	F	00005578	4	4048	4029
X89	F	00005640	4	4086	4067
X9	F	000017C0	4	999	980
X90	F	00005708	4	4124	4105

[illegible]

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	41528	0000- A237	0000- A237
Regi on		41528	0000- A237	0000- A237
CSECT	ZVE7TST	41528	0000- A237	0000- A237

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-16-PackCompare.asm
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**** NO ERRORS FOUND ****